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THESIS

DESIGN AND IMPLEMENTATION OF A ZERO-VOLTAGE-SWITCHING, PULSE-WIDTH-MODULATED, HIGH-FREQUENCY, RESONANT BUCK CHOPPER

by

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September 1999

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ABSTRACT

As the Navy moves toward a modular DC Zonal Electrical Distribution System (DC ZEDS) to reduce both cost and weight over traditional radial shipboard distribution, there is a need to capitalize on technological advances currently available. The 21st century shipboard power distribution system calls for a DC bus architecture to eliminate the need for large transformers and thousands of pounds of cable through the use of high-speed semiconductor converters. In order to realize dramatic reductions in the size and cost of shipboard components through the use of high-speed switches, switch designs must be thoroughly investigated and tested.

This thesis examines the use of soft-switching techniques for use in the future DC-to-DC power converter modules of the DC ZEDS. Soft-switching is analyzed here primarily with a DC down-converter (buck chopper). A low voltage buck chopper is simulated utilizing PSPICE and modeled in the lab. A voltage feedback control algorithm is developed and utilized with the PSPICE model. A comparative study of circuit efficiency is done between a single-source and a two-source soft-switched topology. Finally, recommendations are made for further simulation and modeling to evaluate soft-switching, high-voltage performance capabilities.

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I. BACKGROUND

A. RADIAL ELECTRICAL SYSTEM ARCHITECTURE

Radial electrical distribution is the current method used by naval vessels to reasonably ensure that electrical power is available for vital loads under normal and damage control conditions. Power is transferred throughout the ship via alternating current (AC) passing through a maze of cables. AC generators are placed in strategic positions within the ship to ensure that electrical power generation and distribution is maintained under conditions of battle. Under battle conditions radial electrical distribution allows a vessel to incur damage to one section or generator and still provide power to vital loads by redirecting power flow through undamaged sections. This is made possible by the use of alternate cabling routes. The ship's load is provided with more than one power source through the use of automatic bus transfer devices.

The costs paid for operating with a radial power distribution system are high. No commonalties exist between radial power distribution architectures onboard various different classes of naval ships. This lack of commonality has resulted in unique design requirements each time a ship is built, driving shipbuilding cost higher. Because the design is unique, the ship engineers must be retrained for a different power distribution plant each time they cross deck. Under normal power distribution conditions a ship's load is generally powered by the closest source or determined by generator loading conditions. Because generator loading requires the ability to access loads throughout the ship, cable runs may stretch the entire length of the vessel. Naval ship design requires the division of the ship into as many watertight compartments as possible, reducing the chance of sinking from the force of the sea or the violence of the enemy. Each time a cable passes through a watertight bulkhead the cost of installation rises. The requirement for so many cables, each of which passes through many watertight compartments, dominates electrical plant construction cost. A lower cost distribution system, that is applicable for all classes of ships, is needed. It is high construction cost coupled with the

need for enhanced survivability and reduced manning that is driving the ship building industry from radial architecture toward zonal electrical power distribution design.

B. ZONAL ELECTRICAL SYSTEM ARCHITECTURE

A proposed zonal architecture incorporates two high-voltage Direct Current (DC) buses that run the length of the ship as shown in Figure I-1 [1]. There is one port and one starboard bus, one above and one below the waterline. The architecture is designed to withstand battle damage on the same scale as the radial architecture. No survivable hit will entirely disable the ship's electrical distribution system. The ship is divided into zones corresponding to watertight compartments. The only electrical watertight penetrations are the two DC buses. Within each zone a capability exists to step down the high-voltage DC bus voltage and convert it to AC if necessary from the port and/or starboard bus. This bus architecture is easily incorporated within any class of ship.

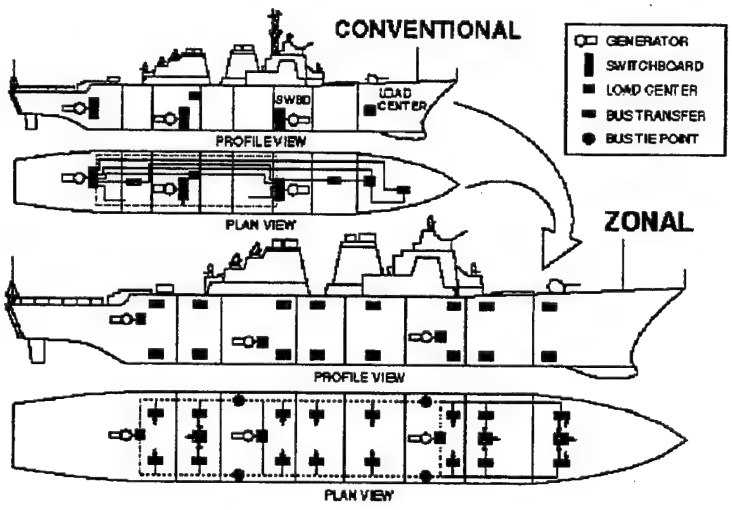

Figure I-1 Radial Architecture vs. Zonal Architecture

The simplicity of a zonal architecture allows straightforward design and minimal cross deck training. Zonal isolation determines what loads are lost, not the path run of a cable, making battle damage assessments quick and accurate. Studies have determined that zonal architecture benefits include significant weight and cost reduction [1]. In addition because high-voltage DC is proposed, further benefits are realized.

C. DC ZONAL ELECTRIC DISTRIBUTION ARCHITECTURE

A reasonable ship service distribution grid will contain three generators for a surface combatant or five generators for a carrier. An example generator could be a twenty-one megawatt, four hundred sixty-volt AC, three-phase, sixty-hertz inter-cooled recuperative gas turbine-driven generator. Such a generator would be appropriate for supplying both ship service and ship propulsion requirements in an electric drive ship. When a multiphase alternator is connected to a controlled rectifier, a high DC bus voltage is realized. A Ship Service Converter Module (SSCM) acts as a buffer between each high-voltage DC bus and each individual powered zone within the ship as shown in Figure I-1 [2]. The SSCM ratings will depend on where it is located in the zone and the load being supplied. The SSCM will provide a regulated output voltage at a reduced level from the applied bus voltage. A solid-state, high-efficiency, high-power, and high-voltage buck chopper is desired to accomplish the mission of the SSCM. A Ship Service Inverter Module (SSIM) will process the lower DC voltage produced by the SSCM and convert it into regulated AC power for use by the zone's AC loads. Mechanical bus transfer switches are replaced with diode logic steering to provide uninterrupted power should one power source fail. Vital loads will utilize both main power busses through diode steering. Transmission lines are kept small by placing a SSCM in each zone that requires power conversion.

ZONAL Electrical Distribution Systems

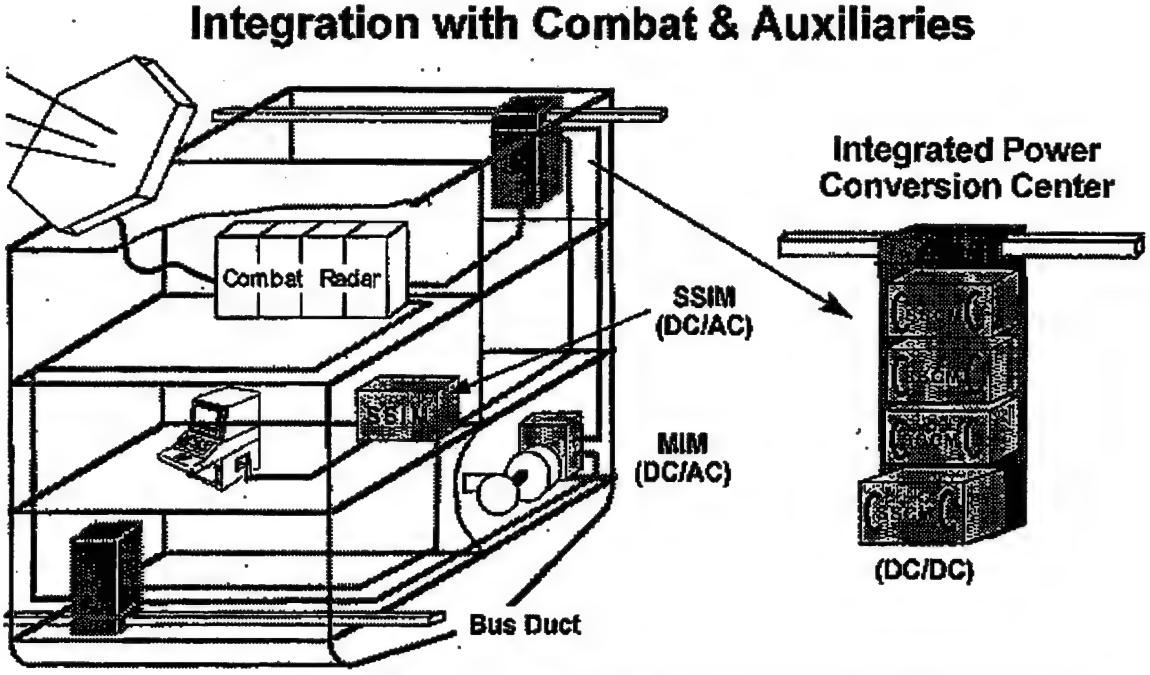

Figure I-2 Basic Zonal Distribution

The DC ZEDS has advantages other than the ones previously discussed. Additional benefits exist because high-voltage DC is used as the mode of electrical power distribution. DC allows faster response to electrical transients. Faster response to electrical transients ensures protection of vital equipment by allowing immediate reaction to overload conditions. Protection circuitry is placed prior to inverters to allow for the use of the faster circuit response time associated with DC. DC permits uncoupling of motor/generator frequencies, allowing optimization of generator/rectifier and motor/inverter size and cost. DC operation makes switchboard paralleling simple for operators. Generators are allowed to operate at their most efficient speeds, reducing fuel cost. DC solid-state breakers only require current flow in one direction and therefore only require one switch as compared to the requirement of two for AC. DC architecture minimizes the number of power conversion steps between source and load. High-voltage operation reduces transmission line size, weight and cost.

Presently, limitations placed on the DC ZEDS are due to the current state of semiconductor technology. Bus voltage is limited to approximately 1500V to 2000V because of the Insulated Gate Bipolar Junction Transistors (IGBTs) and Metal Oxide Controlled Thyristors (MCTs) used in SSCMs. Bus voltage is also limited due to safety concerns regarding an ungrounded system. Currently available devices will handle approximately 1700V blocking, 1200A conduction at 50kHz (experimental). They are fully controllable meaning they can be turned on and off unlike the standard Silicon Controlled Rectifier (SCR). The high-voltage levels desired introduce safety concerns and isolation issues with the SSCMs. The Navy is currently investing in MCTs of the P or N junction variety that are similar to a triac (essentially two SCRs in parallel) with a Field Effect Transistor (FET) on the front end. Only the N_MCT comes close to meeting the required voltage and current handling capability at the switching frequencies desired.

D. POWER ELECTRONIC BUILDING BLOCKS

Power Electronic Building Blocks (PEBBs) are power conversion devices with integrated intelligence. A PEBB will convert any input electrical power to the desired form of voltage, current, and frequency at the output. The PEBB will sense the input power delivered and the output power desired and make the conversions necessary.

The Office of Naval Research (ONR) located in Arlington, Virginia is the primary sponsor of the PEBB program, but industry in general could benefit from PEBBs. Both the Department of Defense (DOD) and global industry could benefit from the reduced design time and cost associated with the use of PEBBs. The PEBB will bring the advantages of modularization and standardization to power electronics.

From the standpoint of the DC ZEDS, the PEBB is the SSIM, SSCM or some combination of the two. A given input power is converted to the desired output values without regard for the demands placed on the device within the design specifications of the module. The design of these modules is broken into a power electronic device, control algorithm, and current and/or voltage sensing technique. Module designs continue to develop as semiconductor device technology advances.

E. THESIS GOALS

The main purpose of this study is to develop and understand a soft-switched resonant converter that will be useful for applications onboard U.S. Naval vessels and within industry. Pulse-Width-Modulated (PWM) converters have been used within industry for years because of their simple topologies and ease of control. The traditional PWM converter switching occurs when there is both voltage across the switch and current available to the switch. This type of converter is dubbed 'hard-switched'. Thus power is lost during each turn-on and turn-off cycle. As power levels and frequency increase, losses escalate.

A converter that may be more useful at high-power levels is called a soft-switch converter. These new converters switch with no voltage across the switch and/or no current through the switch. Thus the only losses that appear are conduction losses. Soft-switching techniques allow the design of more efficient, higher power density systems. This thesis effort will develop and implement a high-frequency DC down-converter that performs power conversions while minimizing conduction losses.

F. CHAPTER OVERVIEW

Chapter II outlines the buck converter and describes the different switching methods currently available. Chapter III contains a description of several of the basic soft-switching topologies and the criteria used to select an optimum topology to implement. A variety of different soft-switching techniques are introduced in Chapter IV. In Chapter V, an analysis of a two-source topology is conducted for later comparison to a single-source topology. A single-source topology analysis is then presented in Chapter VI in a similar manner.

With the initial selection criteria framework introduced, Chapter VI describes the requisites used for the selected soft-switching design and experimental lab results are described. Chapter VII contains a description of the logic control algorithm development

and an analysis of the control algorithm implementation using PSPICE. Conclusions and recommended future research are stated in Chapter VIII.

II. INTRODUCTION TO BUCK CONVERTER OPERATION

A. HARD-SWITCHED STEP-DOWN CONVERTERS

Switching converters utilize controllable switches at frequencies greater than the line frequencies. Figure II-1 illustrates the classic step-down (buck) converter [3]. When the switch is closed, the input voltage is placed across the LC-filter and resistive load. The opening and closing of the switch creates two circuits or modes of operation, assuming that the inductor current remains continuous. Output voltage ripple and inductor current ripple is limited by the inductor capacitor combination. In mode one, Figure II-2a, the switch is activated and the current flows from the source to load. Once the switch is opened (off) load current continues to flow through the freewheeling diode D, therefore mode two is initiated, Figure II-2b. The load current and the output voltage waveforms are illustrated in Figure II-3 for continuous conduction mode [3].

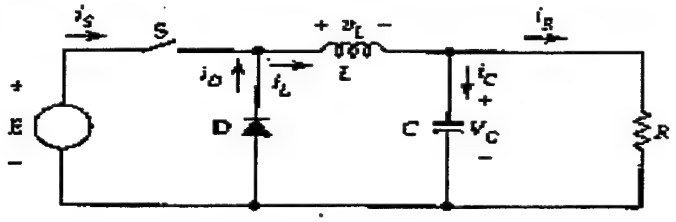

Figure II-1 Basic Buck Converter

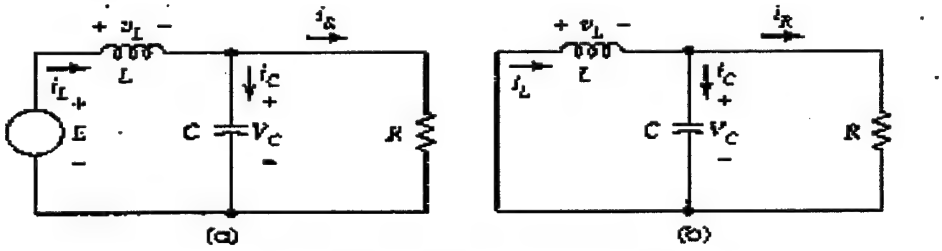

Figure II-2 Basic Buck Converter Modes

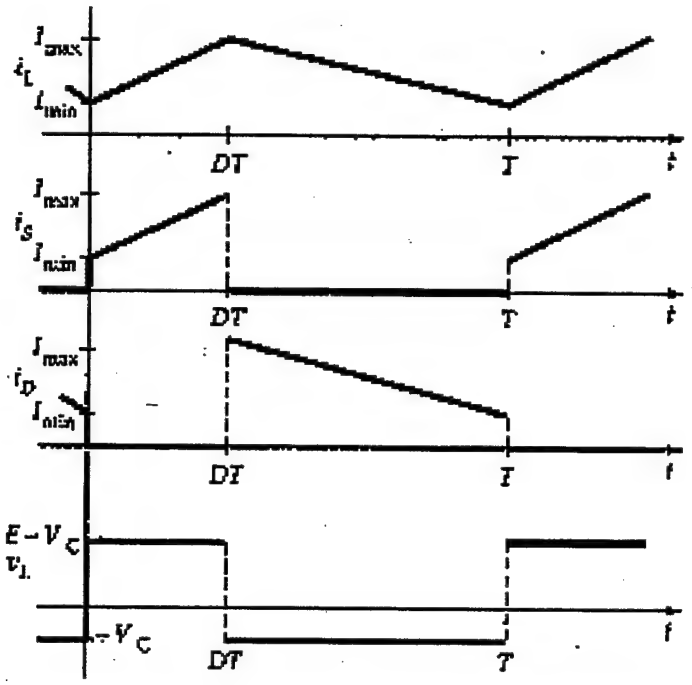

Figure II-3 Basic Buck Converter Waveforms

Because converter switching speeds now range from microseconds to nanoseconds, the "parasitics" inherent to capacitive and inductive elements in converters affect circuit performance. Switching transitions that occur when a voltage differential exists across a switch and current is available to the switch is termed hard-switching. To combat hard-switching the use of snubbing and soft-switching is introduced.

1. Switching Losses

When controllable semiconductor switches are used, some method of control must be utilized. The method of control selected determines the range of switching speeds and the capability to minimize switching stress, loss, and ElectroMagnetic Interference (EMI). Direct control of switching via microprocessor logic signals promotes the control of high-speed switching converters. High-speed switching semiconductor switches have resulted in the development of much smaller, lighter, more efficient, less expensive, and more reliable electronic converters in use today.

Through the use of high-speed switching circuits, a requirement is developed to minimize switching losses, EMI, and current or voltage stresses. Switching losses and EMI occur when a switch is opened or closed under non-zero switch voltage and current conditions. Switching losses are directly proportional to the operating switch. High-speed semiconductor switching devices must be protected from high current or voltage switching conditions in order to prevent damage to the switches and increase system life expectancy. High power requirements force the need for precision switching conditions.

a) Snubber Circuits

Snubbers can be used to minimize large voltages or currents through switches during turn on and turn off to combat switching stress, loss, and EMI. The addition of snubber circuits to the basic converter allows for an increase in switching speed. In the past snubber circuits have been utilized to bring down switching stresses to levels below that of the switch rating. The addition of snubber circuits does however add additional cost and complexity to the existing circuitry and cause additional losses within the snubber elements. The additional cost and complexity must be weighted against the cost and availability of utilizing derated devices.

B. SOFT-SWITCHING

1. Basic Idea

When circuit topologies are able to establish zero difference in the voltage potential across a switch and zero current flow through a switch before and during the instant of a switch opening or closing, the semiconductor device is soft-switching. Resonant and quasi-resonant converters utilize controllable switches which are turned on and/or off during zero-voltage and/or zero-current-switch voltage conditions. The ability to switch under zero-voltage and /or zero-current conditions is called soft-switching. To

minimize switching losses, many soft-switching methods have been published. The selection of soft-switching technique is important when dealing with high power converters.

2. Literature Overview

A number of Institute of Electrical and Electronics Engineers (IEEE) papers have been published in recent years introducing novel soft-switching techniques. A brief overview of many new techniques in order of publication date follows:

- A single-source PWM two-switch topology that achieves zero voltage main switch switching and zero current auxiliary switch switching by using an auxiliary feedback resonant circuit [4].
- A two-source PWM two-switch topology that achieves zero voltage main switch switching and zero current switching with the auxiliary switch [5].
- A single-source, PWM, two-switch topology that utilizes two main switches with one switch operating under zero voltage conditions and a second main switch operating under zero current condition [6].
- A single-source PWM single-switch topology that utilizes voltage clamping to achieve zero voltage switching [7].
- A single-source, PWM, two-switch topology that utilizes control of a resonant inductor period to achieve zero voltage switching conditions on both the main switches [8].
- A two-source PWM two-switch topology that achieves zero voltage main switch switching and zero current auxiliary switch switching [9].
- A second investigation into the single-source PWM two-switch topology that achieves zero voltage main switch switching and zero current auxiliary switch switching of [4] utilizing a higher source voltage [10].

- A single-source, PWM, two-main-switch topology that utilizes control of the resonant inductor period to achieve zero voltage or current switching conditions [11].
- A single-source, PWM, two-switch topology that achieves zero voltage, main switch switching and zero current auxiliary switch switching [12].
- A single-switch, PWM, two-switch topology that achieves zero voltage main switch switching and zero current auxiliary switch switching through the use of a controlled reverse recovery diode [13].

III. SOFT-SWITCHED CONVERTER BASIC COMPARISON

A. OBJECTIVES

The objective here is to examine different methods of achieving soft switching by discussing and analyzing various topologies that have been introduced in recent years. An understanding of basic soft switching and how it can be utilized to meet future design parameters is introduced through specific examples.

In order to draw comparisons and evaluate the candidate topologies, particular operational requirements for a DC-DC converter that is proposed for application in DC ZEDS must be set forth. The following specifications are the minimum requirements set forth for the future high-voltage converter to be built and tested at the Naval Postgraduate School.

1. Specifications

Design specifications call for the following criteria:

- A switching frequency is desired that is > 20 kHz.
- A continuous output power rating of > 10 kW.
- A voltage rating as high as possible utilizing existing Insulated Gate Bipolar Transistor (IGBT) technology.
- Continuous conduction down to 10% of the rated load.
- Full resonant condition at full load.
- Output ripple voltage < 0.5%.

B. SOFT-SWITCHED BUCK CHOPPER TOPOLOGIES

There are two main types of topologies used to create soft–switching conditions for buck chopper circuits. They are the two-source topology and the single-source topology.

1. The Two-Source Topology

Two-source topologies contain two separate voltage sources. Two voltage sources meaning either two actual separate sources or the creation of a second source within a topology. They are designed to provide soft-switching conditions by utilizing their capability to produce canceling voltage potentials across high-speed switches at the instant of switch gating. Several different topologies have been investigated; one is described and analyzed in the next section.

2. The Single-Source Topology

As the name implies single-source topologies operate with a single voltage source. Because they do not require a second supply, they are the most desirable. Most high-power high-voltage applications do not provide the luxury of a second voltage source. Because this thesis desires to implement a low-voltage soft-switching design to serve as a prerequisite for the high-voltage SSCM, a single-source topology is preferred due to the complexity of creating a second internal source. Several different topologies were introduced earlier in Chapter II section B2, Literature Overview. A description of those select single-source topologies with desired and undesired attributes is presented in Chapter IV, Topological Considerations For Design.

C. SELECTION CRITERIA

A soft-switching topology was chosen by first considering the available number of sources. Once the number of available sources is determined the number of devices required to implement a given topology must be considered. The power density requirements of the circuit and the proposed efficiency of the topology are then considered. The efficiency of a given topology can be reasonably compared by determining the number of components directly in the path of main line current flow. Because electrical circuit components such as inductors, resistors, diodes, and switches consume power when active, any such device placed in the main line current path would substantially reduce circuit efficiency. With this idea in mind, topology efficiencies between similar circuits investigated can be rationalized. It is this rationalization that will be used when considering the different topologies available for implementing soft-switching techniques.

IV. TOPOLOGICAL CONSIDERATIONS FOR DESIGN

A. INTRODUCTION

This section investigates several topologies and lists implementation advantages and disadvantages. Owing to the inherent disadvantages, none of the topologies in this section were selected for implementation. After discussing reasons for not selecting the following topologies, detailed descriptions of the most promising candidates for high-efficiency soft-switching topologies are given in later sections.

B. A DESCRIPTION OF A SOFT-SWITCHED BUCK CONVERTER CREATED BY V. GRIGORE, ET AL.

1. Introduction

V. Grigore and J. Kyyra presented a paper in the IEEE Mediterranean Electrotechnical Conference, 1998 entitled "A New Zero-Voltage-Transition PWM buck converter." In their paper they present a new topology capable of being incorporated into a standard buck and other converters. The main objective of Grigore and Kyyra's topology is to establish a converter that operates at high switching frequencies without the switching losses and stresses associated with conventional hard-switching methods. Here the focus is on comparing the new soft-switched buck converter they introduced to a converter that would introduce no new components in the main line current path.

2. General Circuit Description

The topology illustrated in Figure IV-1 builds on the standard buck chopper. Only one source is required and relatively few elements are needed in addition to the standard buck chopper topology. This topology appears to be promising in terms of ease of application to existing converters. The one troubling aspect that is readily apparent is the placement of diode D_2 directly in the main current path. This would suggest a significant decrease in efficiency when compared to a topology that introduces no new components in the main current path.

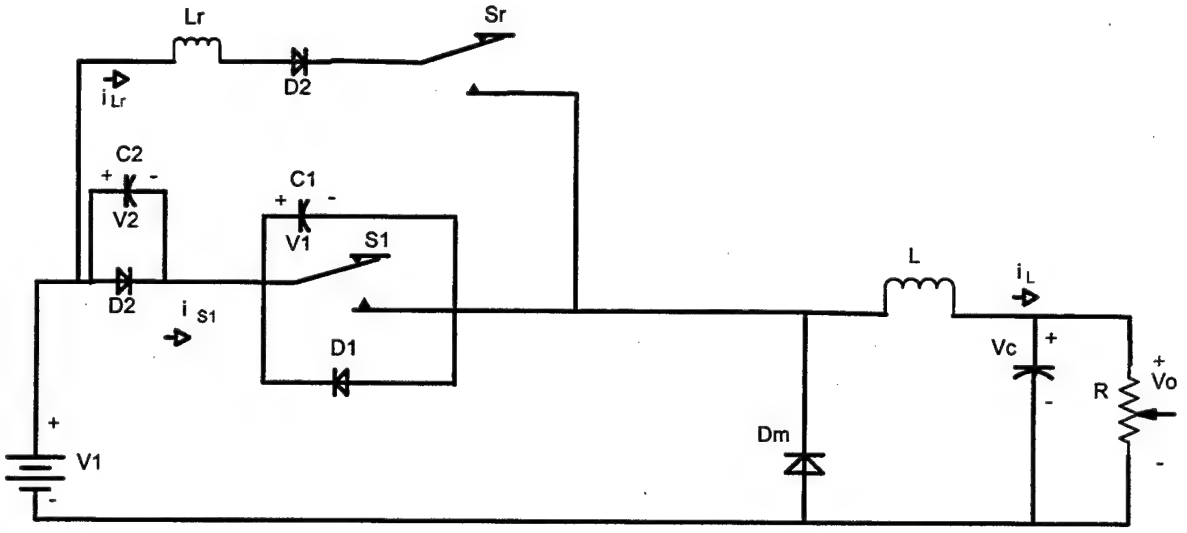

Figure IV-1 Overall Circuit Configuration

Rather than step through the eight modes of operation for this topology and analyze each mode, the published information is used to briefly comment on the expected performance of this topology when compared to a topology that introduces no new components in the main current path.

In reviewing the Grigore and Kyyra paper, it is noted that the main and auxiliary switch gating order facilitates soft-switching. The auxiliary switch is gated first and

undergoes soft-current switching. The main switch turns on under zero voltage conditions and experiences small losses at turn off. The main switch losses are negligible while the auxiliary switch losses are reduced.

3. Conclusions

With the addition of D_2 in the path of the main current flow, the expected efficiency of this circuit is less than the efficiency of a topology that introduces no new components in the main current path; therefore, this circuit is not analyzed further here.

C. A DESCRIPTION OF A SOFT-SWITCHED BUCK CONVERTER CREATED BY H.L. HEY, ET AL.

1. Introduction

Hey, Matias, and Viera presented a paper in IEEE Power Electronics Specialists Conference, 1994 entitled "A Buck ZC-ZVS PWM Converter." In their paper they present a new topology capable of being incorporated into the standard buck converter. The main objective of their topology is to establish a converter that operates at high switching frequencies without the switching losses and stresses associated with conventional hard-switching methods. Here a comparison of the new soft-switched buck converter introduced is made with a topology that introduces no new components in the main current path.

2. General Circuit Description

The Hey, Matias, and Viera topology is illustrated in Figure IV-2. The number of components required to build this soft-switching buck is very small. This topology is promising in terms of ease of application to an existing buck converter. There are two

troubling aspects associated with the topology that are readily apparent. They are the placement of the auxiliary switch, S1, and resonant inductor, Lr, directly in the main current path. This would suggest a significant decrease in efficiency when compared to a topology that introduces no new components in the main current path.

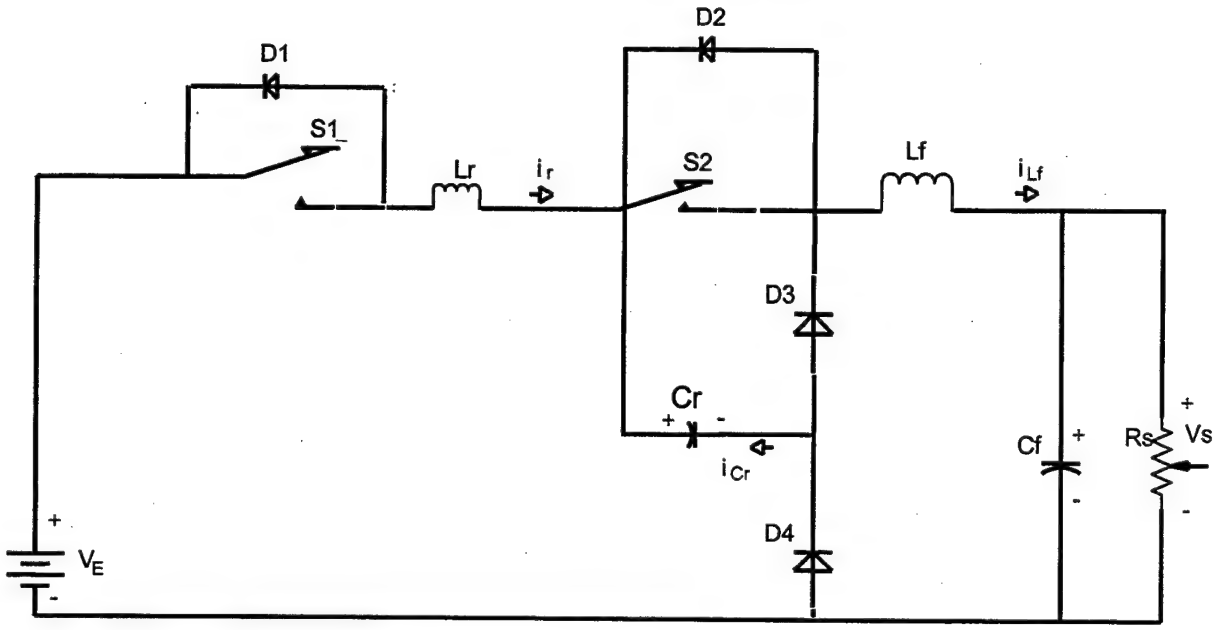

Figure IV-2 Overall Circuit Configuration

Rather than step through the seven modes of operation for this topology and analyze each mode, the published information is referenced to briefly comment on the expected performance of this topology when compared to a topology that introduces no new components in the main current path.

In reviewing the Hey, Matias, and Viera paper, it is noted that the switch gating order for both the main and auxiliary switches is very different from the previous topology. The main and auxiliary switches are closed at the same time. Following through the stages described by the authors, the main current path is diverted through several components in series with the load. This is a very unique approach to soft switching. Although the circuit attains a reduction in actual switching losses, other losses

not normally found in conventional buck choppers are introduced, such as a second inductor (Lr) placed in the main current path. The inductor (Lr) probably introduces insignificant losses, but because it is an additional main path element and the auxiliary switch also exists in the main path, this circuit is not investigated further.

3. Conclusions

This topology offers new methods of reducing switching losses not already seen in the previous topology. The difficulty with this topology hinges on the additional losses that are introduced. Because a second switch and inductor are placed in the main current path, additional losses are introduced to the standard buck topology. These additional losses place this topology in a category of being less efficient than a topology known to have no components in the load current path.

Hey, Matias, and Viera note the introduction of additional losses and introduce an improved version of their topology within their paper. Even with improvements, the resonant inductor, Lr, still remains in the load current path. With the addition of Lr in the path of the load current, the efficiency of this circuit is expected to be less than the efficiency of a topology with no components in the main circuit current path. As a consequence, this circuit is not considered any further.

D. A CONSTANT-FREQUENCY ZERO-VOLTAGE-SWITCHING BUCK QUASI-RESONANT CONVERTER

1. Introduction

P. Dananjayan and C. Chellamuthu presented a paper in IEEE Power Electronics, Drives and Energy Systems for Industrial Growth, 1996 entitled, "A new constant frequency zero voltage switching buck quasi-resonant converter." In their paper they present a new topology capable of being incorporated into the standard buck converter.

The main objective of their topology is to establish a converter that operates at high switching frequencies without the switching losses and stresses associated with conventional hard-switching methods. The following is a presentation of the analysis of the new Quasi-Resonant (QR) soft-switched buck converter they introduced.

Upon initial inspection of Figure IV-3, the soft-switching topology is found to utilize two switches and a resonant inductor in the main current path. Because of this the anticipated output efficiency is expected to be less than stellar. Because of these immediately noted deficiencies in the circuit, efficiency assessment is deferred.

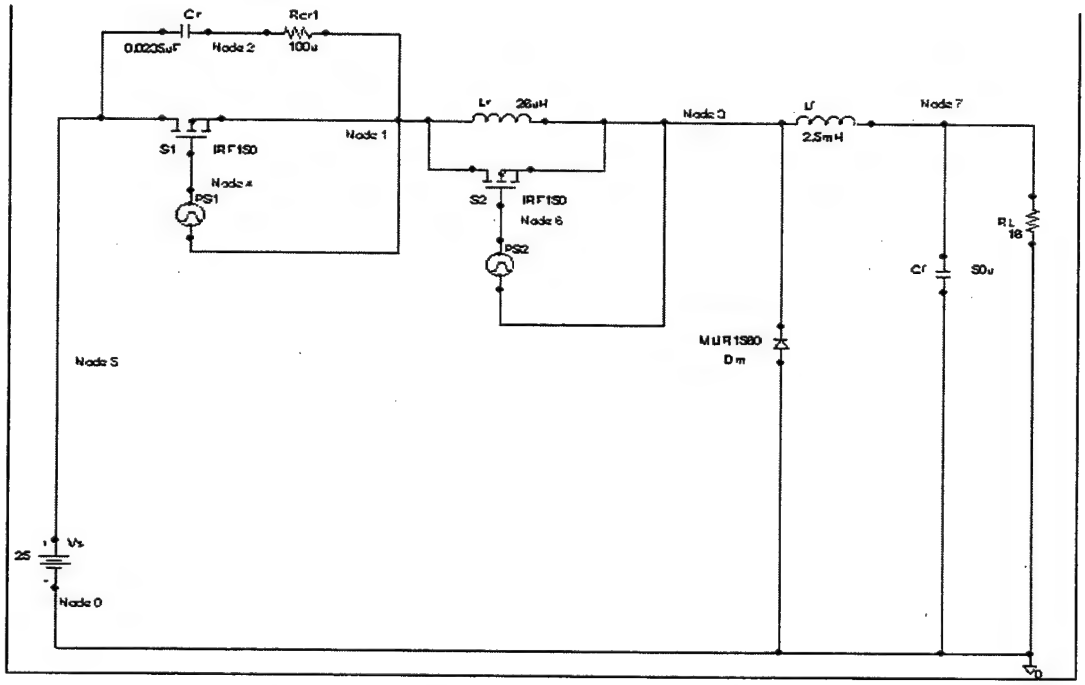

Figure IV-3 Overall Diagram of QR Buck

The goal of this description is to note the improvements to the classic hard-switched buck converter and allow comparisons to be made with other soft-switching topologies, not to develop a converter for a particular use.

This topology works as others do by shaping the device waveforms to produce zero-voltage and current switching conditions. Zero-switching potentials are created by

the established resonance conditions. In the case of quasi-resonant converters, the load must not vary by a substantial amount or the resonant conditions change to a point where zero-voltage switching no longer takes place. Because of the load dependency, this document will not go into depth with circuit analysis of these types of circuits.

2. PSPICE Simulation

Shown in Figure IV-4 is the PSPICE output voltage generated by the quasi-resonant circuit of Figure IV-3. This simulation tests the application of voltage conversion curves provided in the P. Dananjayan and C. Chellamuthu paper. Utilizing their design procedure their results were reproduced here. With the circuit values seen in Figure IV-3, the output voltage in Figure IV-4 was produce. This output voltage approximates their curve-predicted value of 12V for a source voltage between 20 to 25 volts. This is demonstrated here simply to illustrate that such curves can be produced and utilized for possible control purposes.

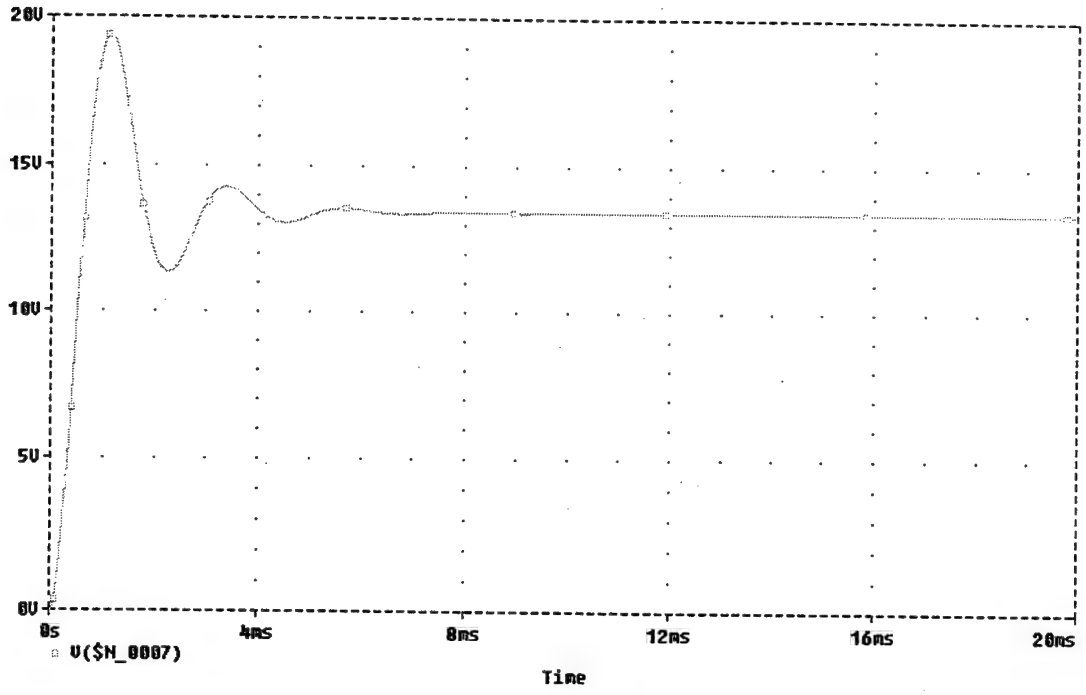

Figure IV-4 Output Voltage

3. Control and Operational Efficiencies

Quasi-Resonant converters are difficult to control for varying load conditions. As a consequence the design of filters and transformers is a difficult task when utilizing this type of converter.

For an efficiency comparison of quasi-resonant converters, the reader is referred to a resonant converter topology presented by K. T. Chau titled "A New PulseWidth-Modulated Zero-Voltage-Switching Multi-Resonant Converter Using Resonant Inductor Freewheeling" [8]. Chau's paper appears in the IEEE Applied Power Electronics Conference and Exposition, 1994. In his paper he presents a quasi-resonant converter exactly like the converter in Figure IV-3 with the addition of a capacitor in parallel with the main diode, D_M. In his paper he presents measured efficiencies in the range of 85% to 95%, depending on the load and supply voltage.

The efficiencies that are found in Chau's experimental results are typical of the quasi-resonant topologies recently presented in many IEEE Proceedings. His circuit

demonstrates improvements in widening load ranges although some range must still exist. Many soft-switching topologies can provide much wider ranges in load handling capability.

This topology presents one of the novel approaches to soft switching. This topology is well suited for constant load applications. Difficulties with control are a factor when dealing with vital loads utilizing a quasi-resonant circuit and they must be addressed. This is because each time a change in load occurs the circuit elements must be adjusted in order to maintain soft-switching conditions.

L.C. de Freitas and P.R. Gomes proposed and presented a solution to the problems mentioned here with quasi-resonant converters. Their buck topology was presented in the IEEE transactions on two separate occasions. Printed once in 1993 and again with further details in 1995. Their topology, shown in Figure IV-5, presents a circuit solution very similar to de Freitas, da Cruz and Farias paper in 1993 entitled "A novel ZCS-ZVS-PWM DC-DC Buck Converter for High Power and High Switching Frequency: Analysis, Simulation and Experimental Results" [5]. However, as in other topologies discussed, the placement of the second switch and resonant inductor is directly in the main circuit path. Placement of these components in the main path will have significant detrimental effects on the high efficiency improvement desired. They do, however, create soft-switching conditions, which allow faster switch operation and longer switch life. They make no claims as to circuit efficiency in their presentation.

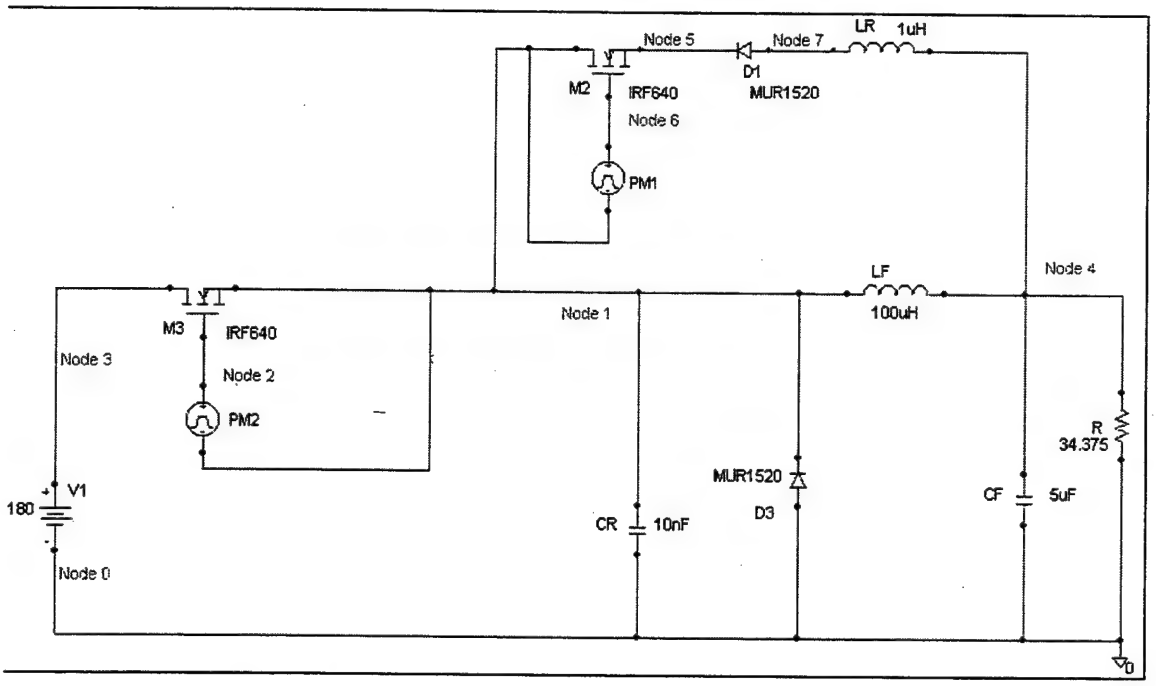

Figure IV-5 de Freita's and Gome's Buck Converter

E. A FAMILY OF SINGLE-SWITCH ZVS-CV DC-TO-DC CONVERTERS

1. Introduction

Takerou Mizoguchi, Takashi Ohgai, and Tamotsu Ninomiya presented a paper in IEEE Power Electronics Specialists Conference, 1994 entitled "A Family of Single-Switch ZVS-CV DC-to-DC Converters" [7]. In their paper they present a new topology capable of being incorporated into the standard buck and many other normally hard-switched converters. The main objective of their topology is to establish a converter that operates at high switching frequencies without the switching losses and stresses associated with conventional hard-switching methods utilizing only a single switch. Here a concentrated effort is placed on describing and analyzing the new soft-switched buck converter they introduced.

Upon initial inspection of the circuit, the soft-switching is attempted with the use of only a single switch within the topology. This initial condition will allow for much easier control as compared to the two-switch configuration introduced in other soft-switching topologies. This topology appears simple in structure. No components are placed in the main current path that may cause an overall decrease in efficiency. The goal of this description is to demonstrate the improvements of the classic hard-switched buck converter and allow comparisons to be made with other soft-switching topologies, not to develop a converter for a particular use.

2. PSPICE Simulation

The circuit to be analyzed is shown in Figure IV-6. The figure represents the configuration utilized in PSPICE. The circuit values were taken directly from the experimental results of the paper presented [7]. Here the circuit performance is simulated in PSPICE and results are presented vice a step-by-step break down of the topology modes of operation. The efficiency of the circuit is a key figure of merit required for later comparison.

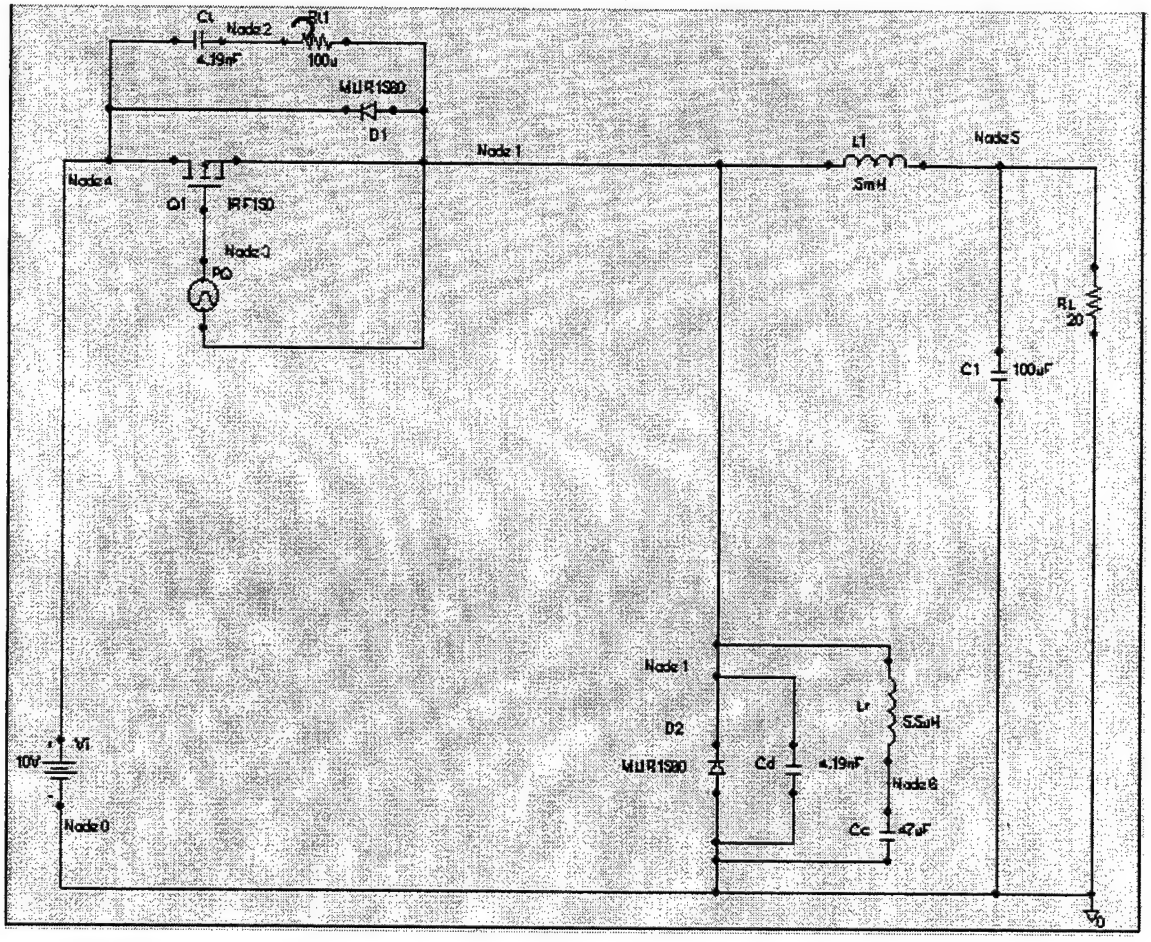

Figure IV-6 Single-Switched, Soft-Switched Buck Topology

Two single-switch topologies were introduced in their paper, but the experimental results were only given for the topology shown in Figure IV-6. Utilizing the given

component values the circuit was simulated. The goal here is to reproduce the experimental waveforms presented in the paper.

The period is set at 5us and duty cycle at 66%. These values were extracted from the given switch experimental voltage waveform. A switch rise and fall time of 25ns was also inserted in the PSPICE simulation to realize real switching conditions. Figure IV-7 illustrates the resultant PSPICE obtained switch waveforms. It is well demonstrated in Figure IV-7 that the switch transitions during zero-voltage conditions. The square marked pulses represent the voltage across the switch while the diamond marked pulses represent the gating signals where the switch is actually opened and closed.

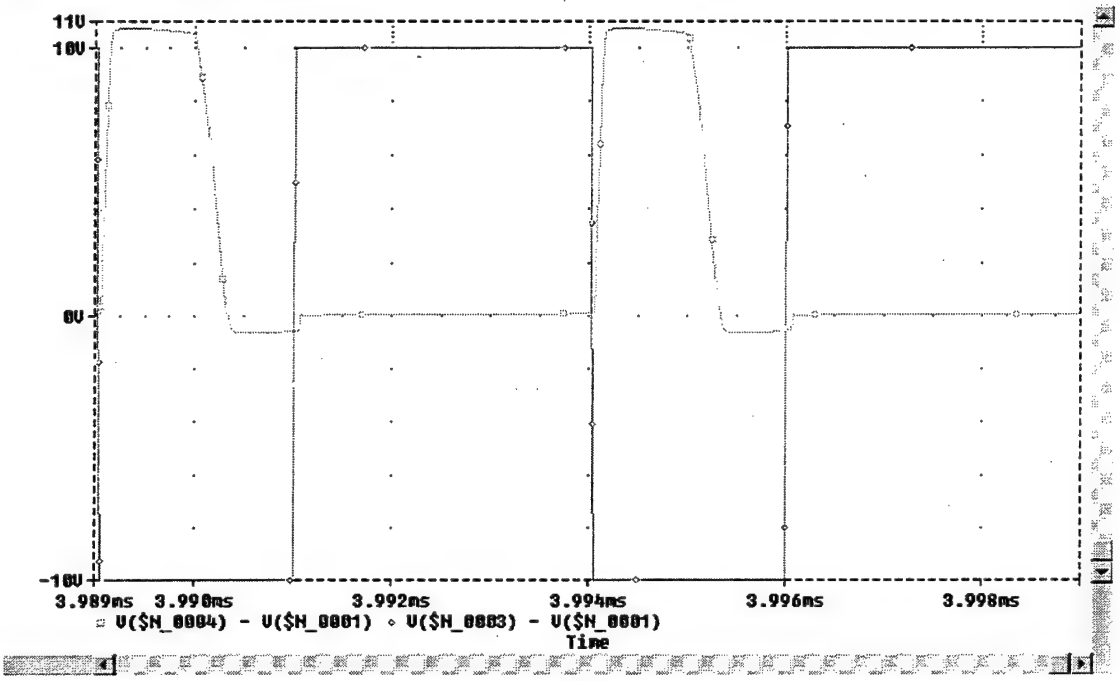

Figure IV-7 Main Switch Voltage and Gating Signal

Next, the main switch current is plotted in Figure IV-8. This is very similar to the waveform presented in the paper. There appears to be more detail with regard to the negative going pulse when the switch is opened. The voltage across Q1 is slightly negative in Figure IV-7 when Q1 is switched on. The paper contends it is switched at exactly zero voltage with the same given component values. Because the PSPICE

simulation is only demonstrating a difference of less than 0.5 volts, it is the author's contention that the results match.

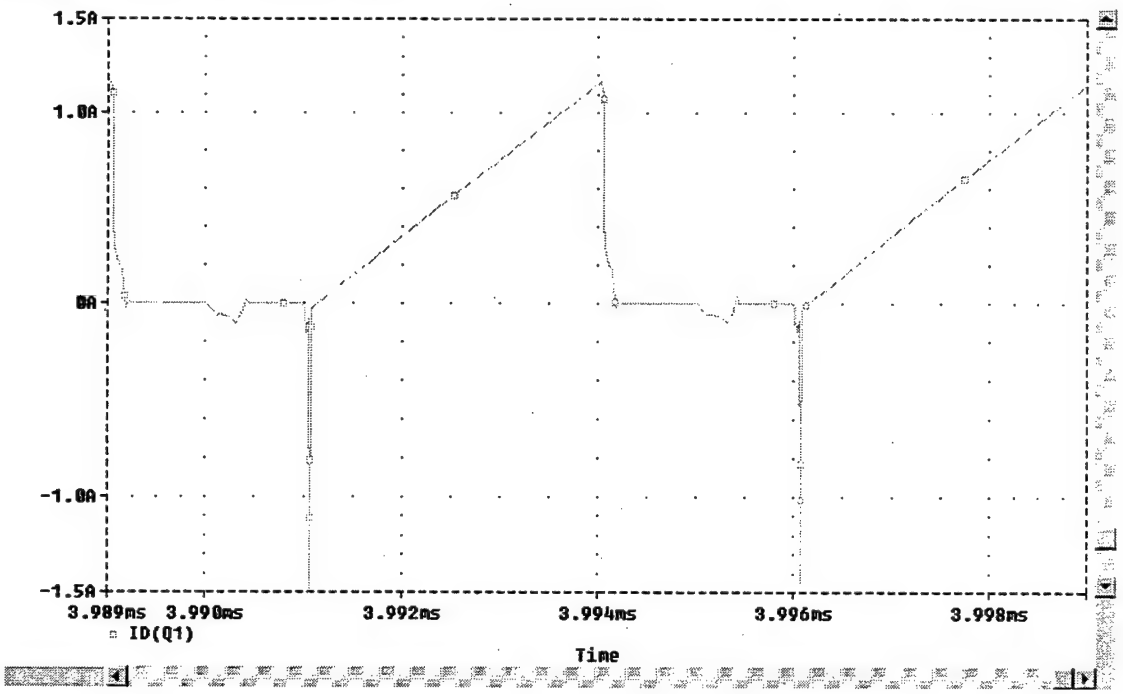

Figure IV-8 Main Switch Current

Figure IV-9 illustrates the resonant inductor current obtained from the PSPICE simulation. The inductor current resonant condition peaks are at +/- 0.75A. This simulation waveform matches the given experimental results.

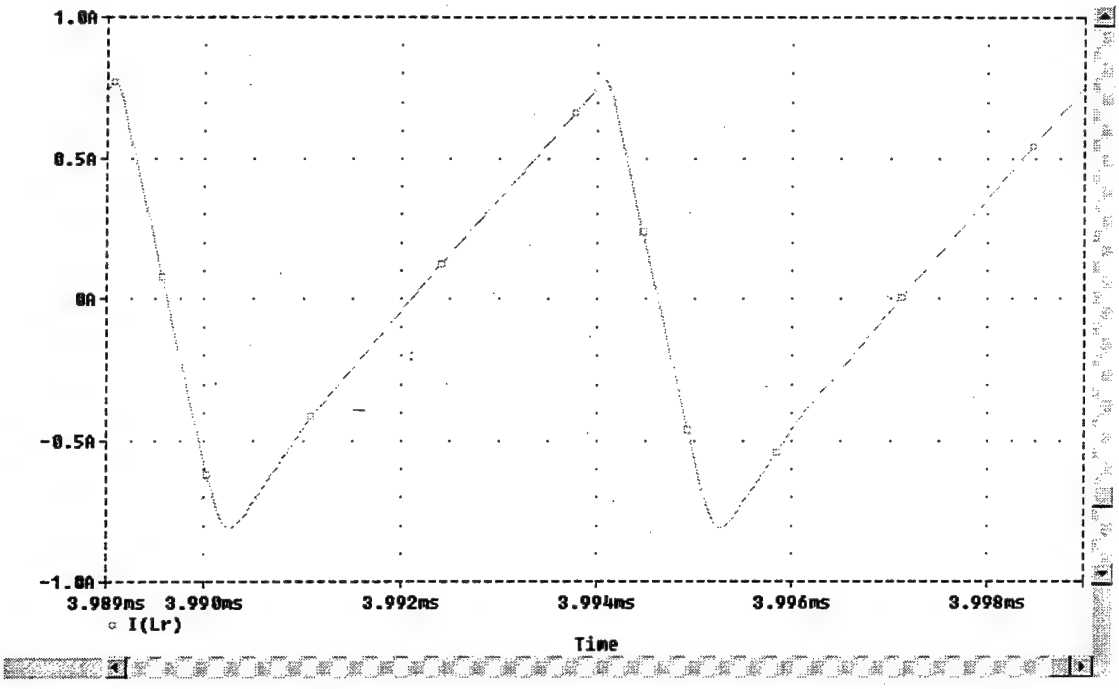

Figure IV-9 Resonant Inductor Current

Figure IV-10 represents the current flow through the diode, D2. Again the PSPICE waveforms match the given experimental results. These waveforms are simply utilized to confirm that the PSPICE simulation produced results that match the reference papers output. With this confirmation the efficiency values found next are reasonably assumed accurate.

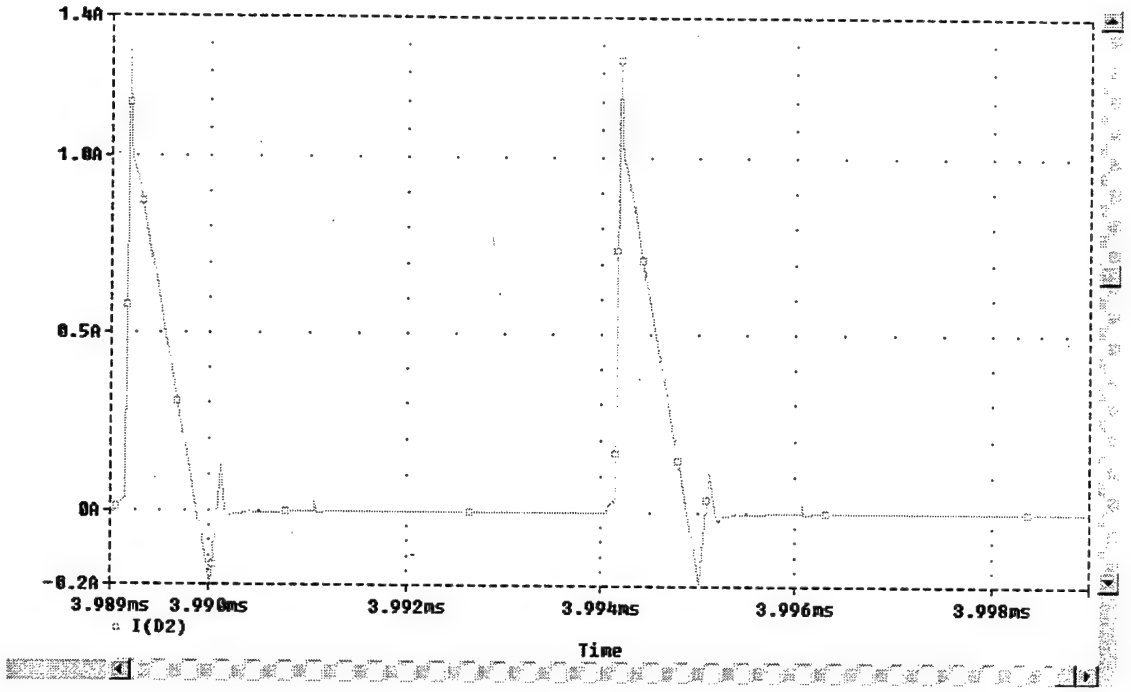

Figure IV-10 D2 Current

By using the simulation from PSPICE, an efficiency value was obtained for comparison with the other candidate circuits. The efficiency of the circuit was obtained by simply dividing the output power by the input power. From Figure IV-11 the efficiency is found to be 88.1% after a 20ms simulation. As seen, the efficiency increases to a constant value approximately 20ms after startup. Because this circuit only utilizes one switch, the benefits of a single switch may out weigh the few percentage points in efficiency improvement seen in the two-switch topologies analyzed here. This circuit warrants further consideration because of its single-switch topology. At higher voltage and current levels efficiency may prove the dominant factor in a soft-switching topology selection.

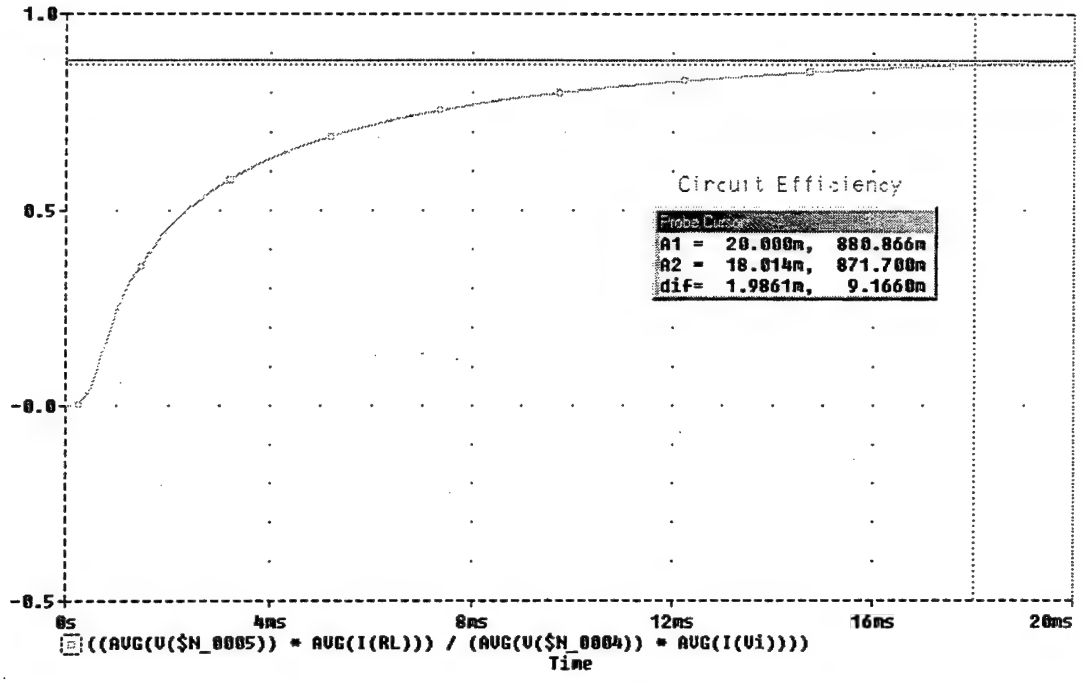

Figure IV-11 Circuit Efficiency

In Figure IV-12 the main inductor current, I_{L1}, is illustrated in order to confirm whether or not the circuit is operating in continuous current conduction mode. Since the current does not go to zero, continuous conduction is maintained.

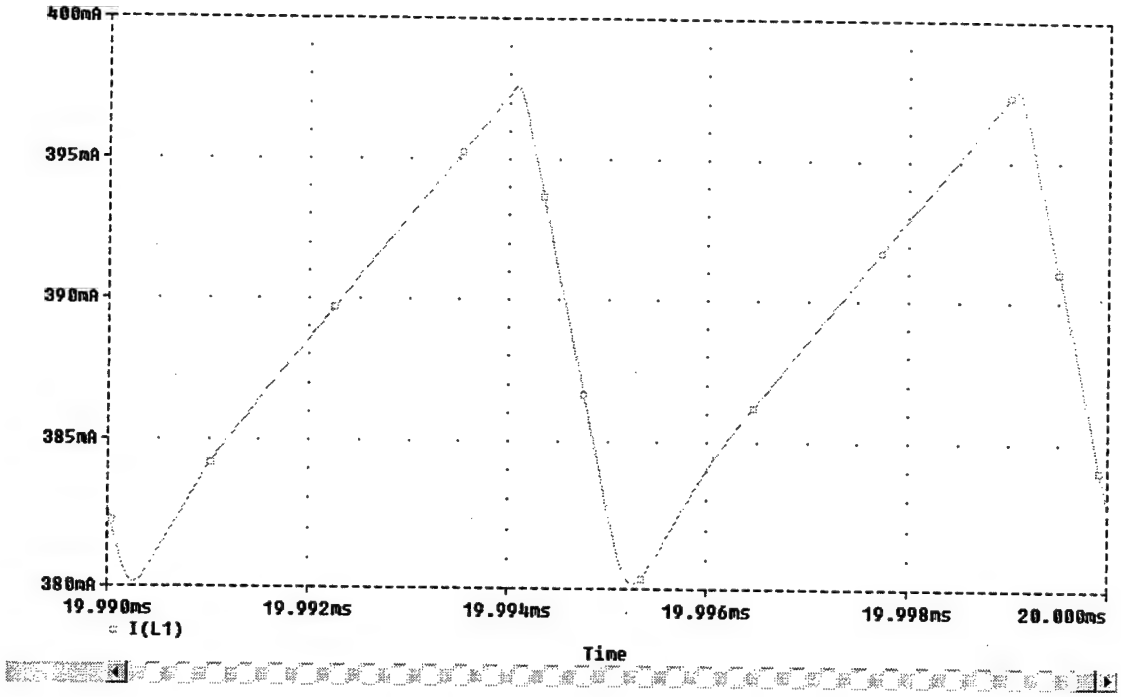

Figure IV-12 Main Inductor Current I_{L1}

Figure IV-13 is an illustration of the converter output voltage. The output voltage shown is approximately 7.8V. A classical hard-switched buck chopper with input voltage = 10V, load of 20 ohms, and a 66% duty cycle has the following load voltage, (D)(Vi) = V_L = 6.6V. The output voltage does differ from the classical buck circuit. The difference is due to the addition of the resonance circuits established around Q1 and D2. The reference paper does give an output voltage conversion equation for predicting the expected output based on the original buck circuit values. They obtained the equation by solving the state equations for the output voltage.

Realizing that at such low voltage and current levels, efficiencies are difficult to confirm. In order for this circuit to be directly compared to other selected topologies a higher voltage circuit must be constructed and tested.

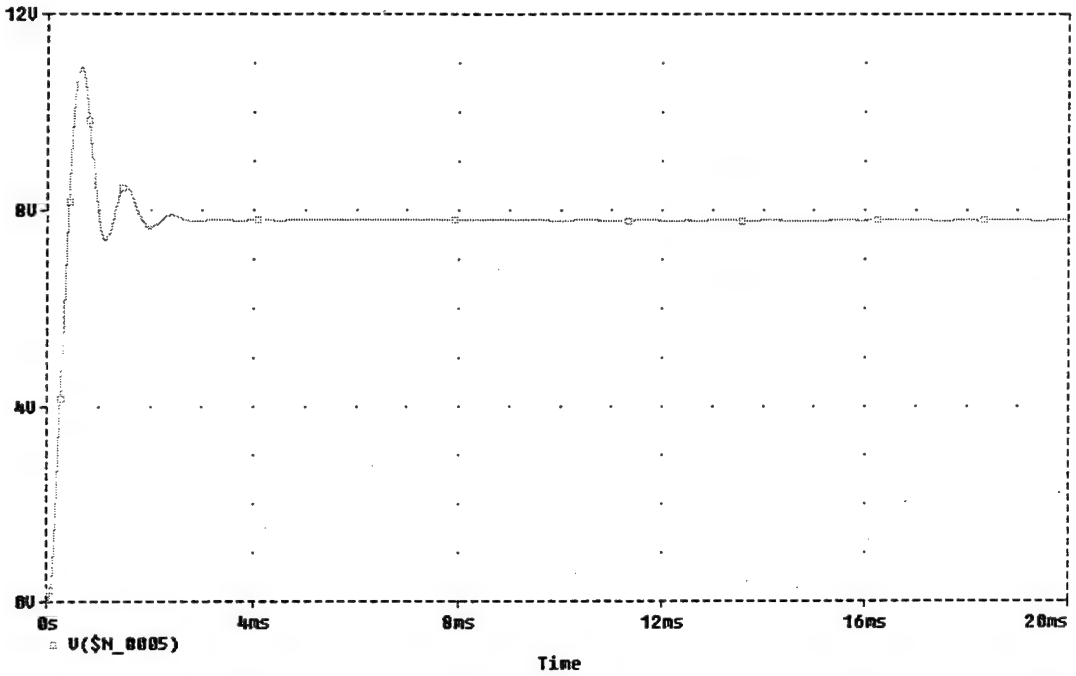

Figure IV-13 Load Voltage

Overall this topology presents a very interesting approach to soft-switching. This topology is well suited for low voltage and current applications. High volume production could benefit from the minimum component requirements for implementation. Conversion of existing, classical hard-switching buck converters to this topology is a valid option.

In the next chapter a look at similar methods of developing soft switches is made when two sources are available. A two-source topology exists whether the second source is generated within the topology or an actual second source is introduced.

V. ANALYSIS OF A SOFT-SWITCHED TWO-SOURCE TOPOLOGY

A. INTRODUCTION

Ricardo Nederson Prado presented a paper in IEEE Power Electronics Specialist's Conference, 1994 entitled "A New ZVT PWM Converter Family: Analysis, Simulation and Experimental Results" [9]. In his paper he presents a new topology capable of being incorporated into standard buck and many other normally hard-switched converters. The main objective of Prado's topology is to establish a converter that operates at high switching frequencies without the switching losses and stresses associated with conventional hard-switching methods. Details of the circuit operation and characteristics are presented in this section.

Upon initial inspection of the circuit, note that the source is divided into two sources. This limits the application of this particular topology to such systems that must supply two sources or generate a second source from within the topology. The goal of this section is to demonstrate improvements in the classic hard-switched buck converter and allow comparisons to be made with other soft-switching topologies, not to develop a converter for a particular use. The method for developing the modeling equations for this topology comes from earlier work performed at the Naval Postgraduate School [14].

B. PRINCIPLE OF OPERATION

The circuit to be analyzed is shown in Figure V-1. A resistive load has replaced the constant-power current source load in Prado's topology. The load was chosen so that comparisons could be made with other topologies. The main inductor, L, is selected to be at least 10 times larger than the resonant inductor, Lr. The goal of the overall soft-switching buck circuit is to create conditions within the circuit that will allow the main switch, Q, to be opened and closed during zero-voltage transitions (ZVT). Similarly, soft-switching conditions for the auxiliary switch, S1, must be created. However, this

circuit does not create the optimum switching conditions (i.e. zero voltage switching) for S1, but it is able to create soft-current-switching conditions as described later.

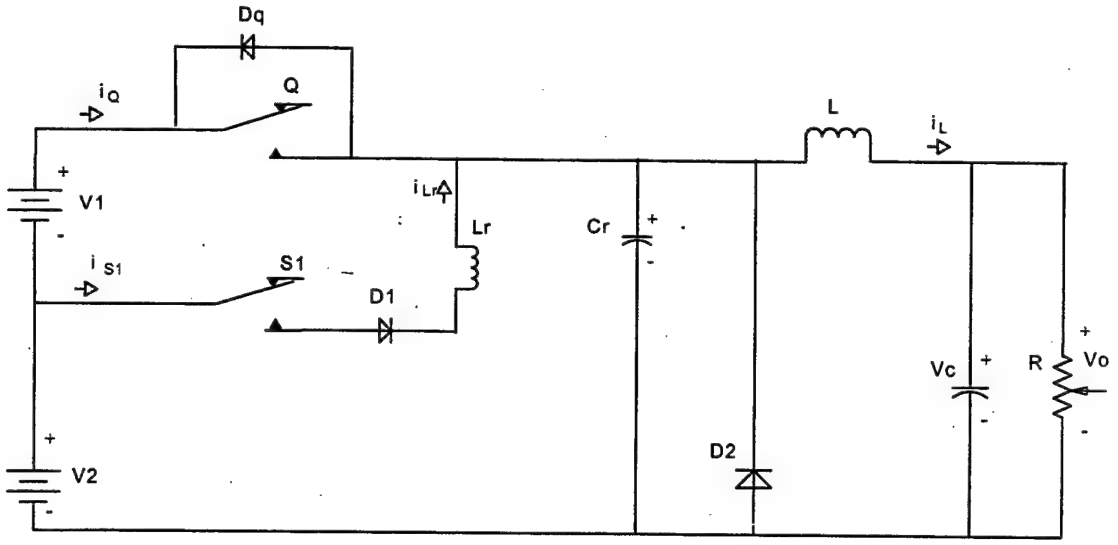

Figure V-1 Two-Source Soft-Switched Buck Topology

Beginning with Mode 1 and stepping through each of the six modes, the conditions around each switch are noted. To simplify the circuit analysis, it is assumed that the circuit operates in steady state and all power devices are ideal.

The first mode of operation (Mode 1) is depicted in Figure V-2. The main and auxiliary switches are open, the inductor current, i_L, is being transferred to the load, and the main diode, D_2, is conducting. The output capacitor voltage, V_c, is at a steady-state regulated value, $V_c = D\,(V_1+V_2)$, where D is the duty-cycle. Capacitor C_r is completely discharged, $V_{Cr} = 0V$, and there is no current flowing in the resonant inductor, L_r, therefore $i_{Lr} = 0A$. During this mode the inductor current, i_L, will decrease at a constant rate from $i_{L\,max}$ to i_{Lmin}. The main inductor's minimum current, i_{Lmin}, occurs at the instant before the auxiliary switch, S_a, is closed and Mode 2 begins. The time frame for Mode 1 is measured by the amount of time that both switches remain open simultaneously.

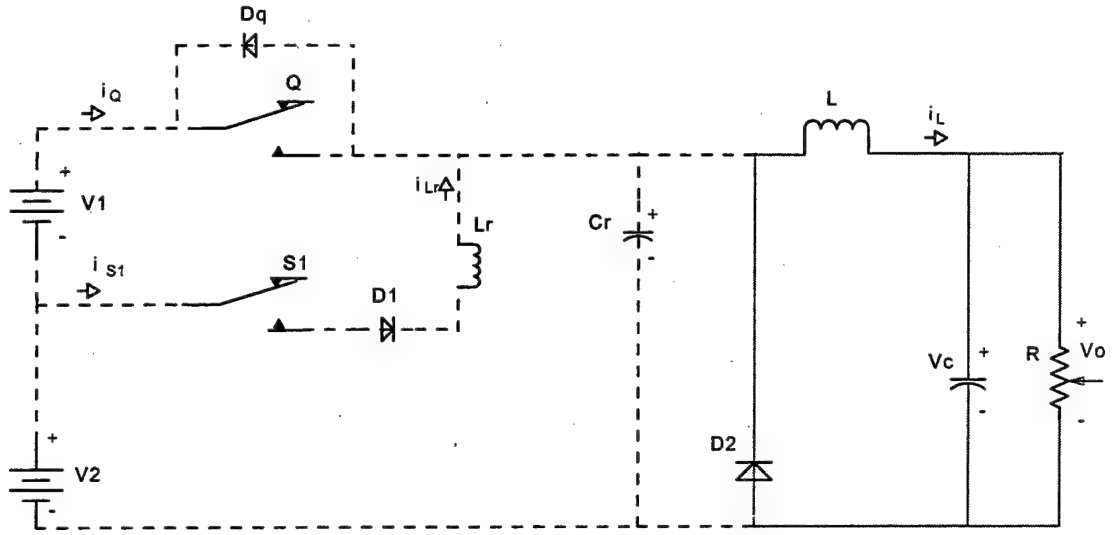

Figure V-2 Mode 1

The second mode of operation (Mode 2) begins when the auxiliary switch, S_a, is closed as illustrated in Figure V-3. Under this condition, S_1 is closed with a potential of approximately V_2 across it, but switch current, i_{s1}, is zero. This means no switching loss occurs in S_1. Because i_{s1} increases gradually at a rate equal to the rate of change found in i_{Lr}, given by $\frac{d}{dt} i_{Lr} = \frac{V_2}{L_r}$, the switching is referred to as soft switching under zero-current conditions. Initially as S_1 is closed D_2 is still conducting. This condition places the source voltage, V_2, across L_r, making $V_{Lr} \cong V_2$. Since $\frac{d}{dt} i_{Lr} = \frac{V_2}{L_r}$, the resonant inductor current, i_{Lr}, increases rapidly until $i_{Lr} = i_L$ where i_L is still quite close to $I_{L,min}$, provided V_2/L_r is large. This condition starves the main diode, D_2, of current causing it to naturally turn off and end Mode 2.

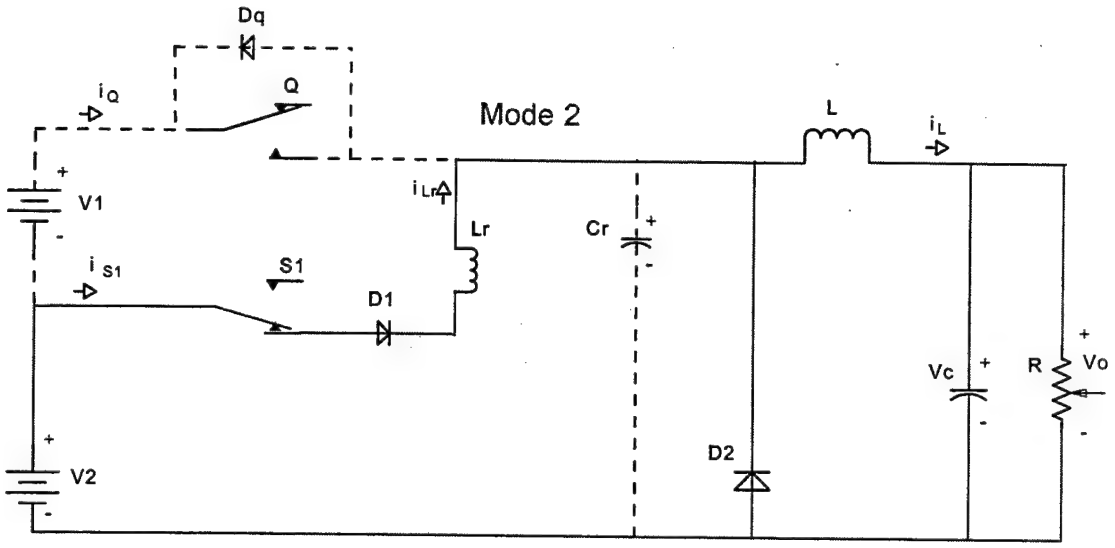

Figure V-3 Mode 2

In the third mode (Mode 3), a resonant condition exists between C_r and L_r that is illustrated in Figure V-4. V_{Cr} and I_{Lr} change in a resonant manner until $V_{Cr} = V_2$. With S1 closed the voltage potential across the main switch is given by $V_Q = V_2 - V_1$. If $V_2 = V_1$ then $V_Q = 0$ and a zero-voltage condition has been created across the main switch, Q. Mode 3 ends when Q is closed.

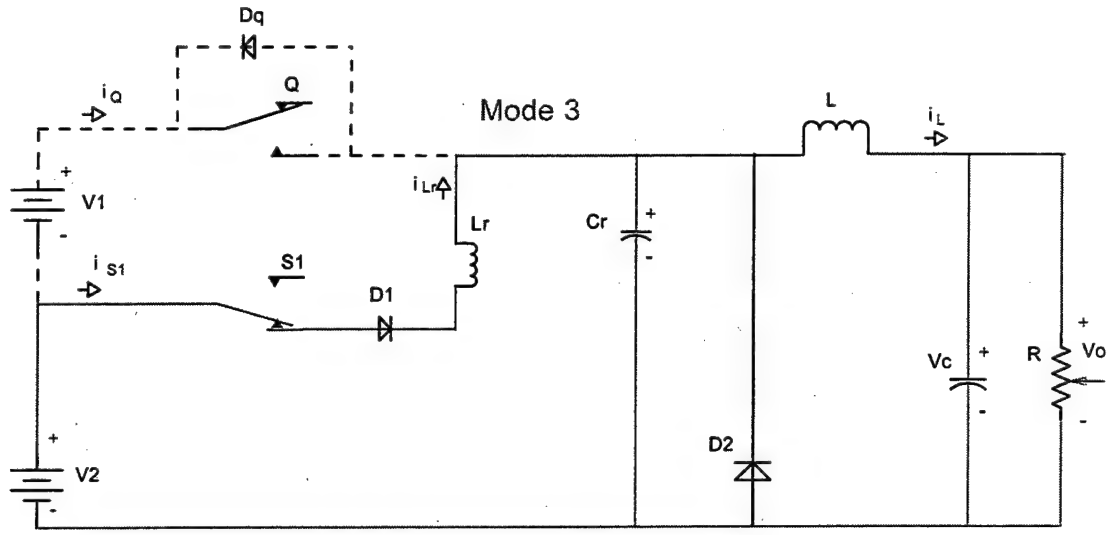

Figure V-4 Mode 3

The fourth mode (Mode 4) begins when the main switch, Q, is closed with V_Q at approximately zero volts, therefore zero-voltage switching is realized across the main switch as depicted in Figure V-5. Because the voltage potential across V_{Lr} is approximately zero if $V_1 = V_2$, the resonant inductor current, i_{Lr}, decreases linearly with time. The voltage drop across the closed auxiliary switch, S_1, is approximately zero. Given $V_1 = V_2$, S_1 may now be opened.

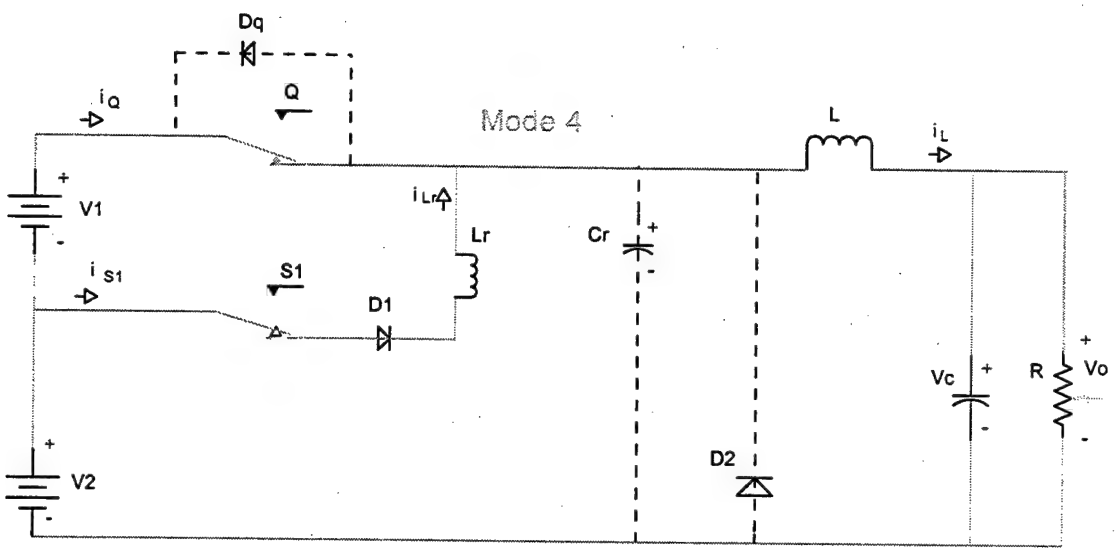

Figure V-5 Mode 4

The fifth mode (Mode 5) begins when the auxiliary switch, S_1, is opened. V_{Cr} must increase to $(V_1 + V_2)$ volts. The circuit current flow exists as depicted in Figure V-6.

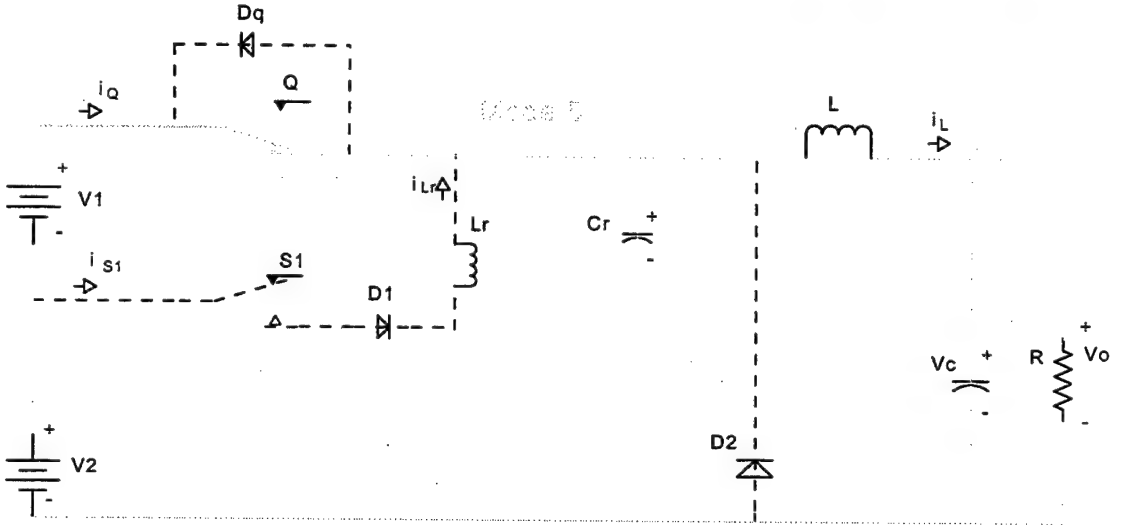

Figure V-6 Mode 5

The next mode (Mode 6) begins when $V_{Cr} = V_1 + V_2$. Once $V_{Cr} = V_1 + V_2$, the circuit current flow is as depicted in Figure V-7. Q has assumed the load current I_L and this mode remains active until Q is opened.

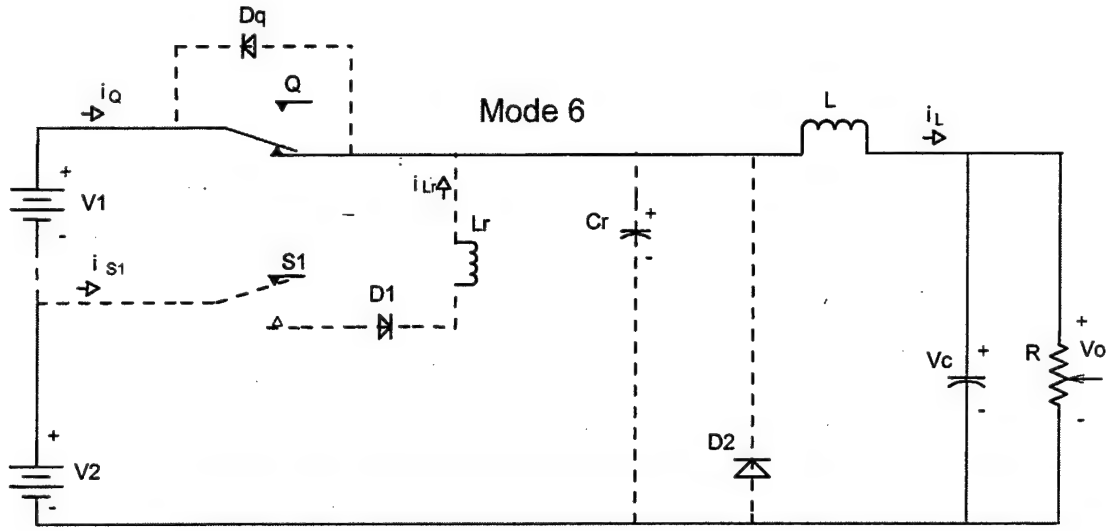

Figure V-7 Mode 6

The seventh and final mode (Mode 7) begins the instant the main switch, Q, is opened. When Q is opened, the current i_L must remain continuous and therefore will flow through C_r. This current path is shown in Figure V-8. V_{Cr} decreases linearly with time to zero. If the load is small, capacitor Cr may not completely discharge. If a light-load condition exists, then the circuit must be operated with $V_2 > V_1$ to ensure C_r is completely discharged in order to operate under soft-switching conditions.

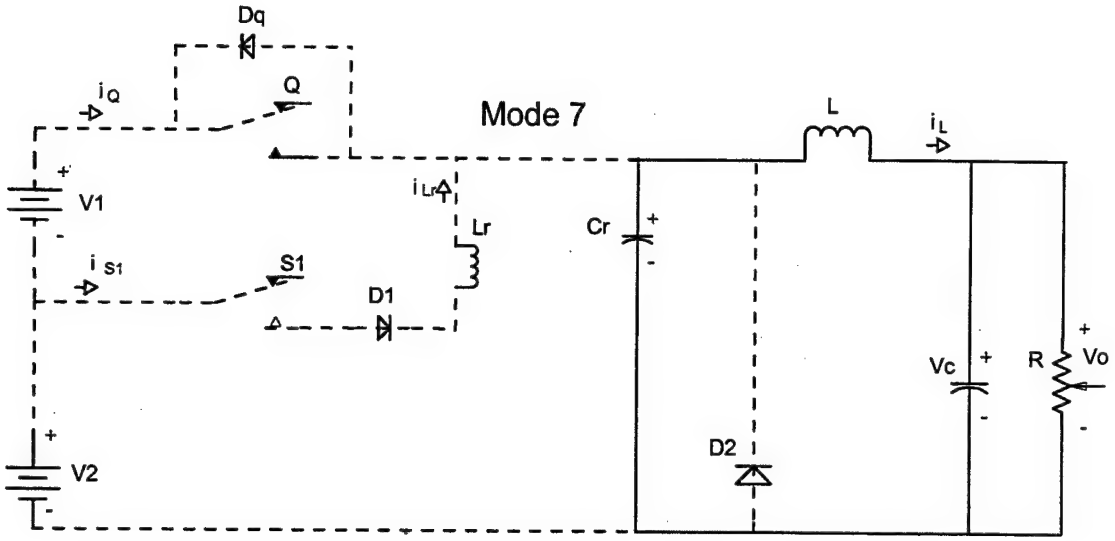

Figure V-8 Mode 7

At this point D_2 is forward biased and begins to freewheel; therefore, Mode 1 is re-initiated. The next steady-state switching cycle is now ready to begin.

C. DYNAMIC MODELING OF MODES

Each of the six modes of operation previously described is governed by a set of differential equations prescribed by the circuit configuration. The transitions between modes are specified by conditions on the network state variables. This section documents the state equations for each mode and sets forth each transition constraint.

For the circuit under consideration, the state variables correspond to the currents or voltages of the four energy storage elements. In particular, i_L, V_c, V_{Cr}, and i_r are the state variables. All equations are derived assuming zero switch and diode conduction drops, ideal inductors and capacitors, and stiff dc input voltage sources. The following equations describe the corresponding dynamics for each mode.

1. Mode 1

The dynamics shown below are derived from the Mode 1 circuit depicted in Figure V-2.

$$\frac{d}{dt}i_L = -\frac{V_c}{L} \tag{5-1}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{5-2}$$

$$\frac{d}{dt}i_r = 0 \tag{5-3}$$

$$\frac{d}{dt}V_{Cr} = 0 \tag{5-4}$$

Any initial conditions are attained from the end of Mode 6. Transition to Mode 2 begins when a gating signal is applied to the auxiliary switch, S_1. The gating signal is

synchronized with the clocking signal used to activate the main switch, Q, described later in Mode 4.

2. Mode 2

The dynamics shown below are derived from the Mode 2 circuit depicted in Figure V-3.

$$\frac{d}{dt}i_L = -\frac{V_c}{L} \tag{5-5}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{5-6}$$

$$\frac{d}{dt}i_r = \frac{V_2}{L_r} \tag{5-7}$$

$$\frac{d}{dt}V_{Cr} = 0 \tag{5-8}$$

These equations govern circuit operation up until $i_r = i_L$. Once $i_r = i_L$ the circuit has transitioned into Mode 3.

3. Mode 3

The dynamics shown below are derived from the Mode 3 circuit depicted in Figure V-4.

$$\frac{d}{dt}i_L = \frac{V_{Cr} - V_c}{L} \tag{5-9}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{5-10}$$

$$\frac{d}{dt}i_r = \frac{V_2 - V_{Cr}}{L_r} \tag{5-11}$$

$$\frac{d}{dt}V_{Cr} = \frac{i_r - i_L}{Cr} \tag{5-12}$$

The initial condition on V_{Cr} is approximately zero volts as diode D_2 constrains V_{Cr} from charging in Mode 2. When D_2 turns off, V_{Cr} charges to approximately V_2 at the rate given by (5-12). Since (5-12) is dependent on the two inductor currents which are in transition, a resonant circuit exists until $V_{Cr} = V_2$. At this point the circuit is ready to transition into Mode 4. V_{Cr} must be monitored for this condition in order for the circuit to correctly transition to Mode 4 with a zero voltage potential across the main switch, Q.

4. Mode 4

Mode 4 is initiated when either $V_{Cr} = V_1$ (if that condition is used in the control) or when the main switch is closed as dictated by the duty-cycle control. The dynamics shown below are derived from the Mode 4 circuit depicted in Figure V-5.

$$\frac{d}{dt}i_L = \frac{V_2 + V_1 - V_c}{L} \tag{5-13}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{5-14}$$

$$\frac{d}{dt}i_r = \frac{V_1}{L_r} \tag{5-15}$$

$$\frac{d}{dt}V_{cr} = \frac{i_r + i_Q - i_L}{Cr} \tag{5-16}$$

The current through the main switch is given by:

$$i_Q = i_L + i_{Cr} - i_r \tag{5-17}$$

Mode 4 ends when $i_{Lr} = 0$.

5. Mode 5

Mode 5 is initiated when the auxiliary switch, S_1, is turned off. The turn off may be specified based on some sensed variable or based simply on a timing criterion (more on this later). The dynamics shown below are derived from the Mode 5 circuit depicted in Figure V-6.

$$\frac{d}{dt}i_L = \frac{V_1 + V_2 - V_c}{L} \tag{5-18}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{5-19}$$

$$\frac{d}{dt}i_{Lr} = 0 \tag{5-20}$$

$$\frac{d}{dt}V_{Cr} = \frac{i_Q - i_L}{Cr} \tag{5-21}$$

These dynamics govern to the point where V_{Cr} increases to $V_1 + V_2$. The circuit then transitions to Mode 6.

6. Mode 6

Mode 6 is initiated when $V_{Cr} = V_1 + V_2$. The dynamics shown below are derived from the Mode 6 circuit depicted in Figure V-7.

$$\frac{d}{dt}i_L = \frac{V_1 + V_2 - V_c}{L} \tag{5-22}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{5-23}$$

$$\frac{d}{dt}i_{Lr} = 0 \tag{5-24}$$

$$\frac{d}{dt}V_{Cr} = 0 \tag{5-25}$$

The Main Switch, Q, assumes the full load current.

7. Mode 7

Mode 7 is initiated when Q_1 is turned off. The dynamics shown below are derived from the Mode 7 circuit depicted in Figure V-8.

$$\frac{d}{dt}i_L = \frac{V_{Cr} - V_c}{L} \tag{5-26}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{5-27}$$

$$\frac{d}{dt}i_{Lr} = 0 \tag{5-28}$$

$$\frac{d}{dt}V_{Cr} = \frac{i_L}{Cr} \tag{5-29}$$

V_{Cr} will decrease linearly to zero at which time D_2 is forward biased and begins to conduct. This places the circuit back in Mode 1 with the current freewheeling through D_2.

This section has set forth the dynamic equations for the individual modes together with the transition conditions. The next section utilizes the equations derived here and a PSPICE simulation to model the Prado topology with selected circuit specifications.

D. PARAMETER DESIGN

For the given topology, the design engineer must select four component values: the main inductance, L, the main output capacitance, C, the resonant inductance, L_r, and the resonant capacitance, C_r. In addition, the designer must specify the switching frequency and establish the criteria for turning the auxiliary switch, S_1, off. A control algorithm must be formulated and suitable diodes selected for the network. One item that has thus far been overlooked is the diode directly across the main switch, Q. If $V_1 < V_2$, a

new mode is introduced where the diode conducts the difference in $i_L - i_{Lr}$. This case is not simulated here.

The basic design of a buck chopper described earlier is briefly highlighted next. For convenience, the following specifications are assumed: the input voltage, $V_1 = V_2$ is fixed at 25.4V, the desired output voltage, V_{out}, is 30V, the rated output load is 46.6W, the switching frequency is set at 2kHz, and the output ripple should be less than 0.1V. The main inductor is sized principally to ensure that the converter remains in the continuous current conduction mode for all loads greater than 10% of rated (R_{rat} = 19.31 ohm). With the nominal duty-cycle given by

$$D_o = \frac{30V}{50.8V} = 0.5906 \tag{5-30}$$

and the load resistance at 10% power given by:

$$R_{crit} = 10R_{rat} = 193.1\Omega, \tag{5-31}$$

the critical inductance is found to be:

$$L_{crit} = \frac{R_{crit}}{2f_s}(1 - D_o) = 19.8mH \tag{5-32}$$

where f_s is the switching frequency in Hz. The main inductance is assumed to be L = 42.5mH to ensure continuous conduction mode. Next, the minimum capacitance is estimated from the following steady-state ripple constraint:

$$C_{\min} = \frac{D_o}{8Lf_s^2 \Delta V_{out}}(V_1 + V_2 - V_{out}) = 90.3\mu F \tag{5-33}$$

V_{out} is an assumed peak-to-peak output ripple of 0.1V. The actual selection of the capacitor is strongly influenced by the control loop design. If C is selected too small then there is insufficient energy in the capacitor to maintain the output voltage during a transient. If C is selected too large then small variation in the output voltage results in the duty cycle bouncing between full on and full off. This occurs because there is too much

energy in the capacitor compared to what the inductor can handle. In this case, it is postulated that C = 200μF yields a good compromise between available energy for transients and dynamic range in the control loop.

For rated load, it is also of interest to quantify the expected ripple current. The minimum steady-state inductor current is found to be

$$I_{L\min} = \frac{V_{out}}{R_{rat}}\left[1 - \frac{R}{2Lf_s}(1 - D_o)\right] = 1.48A \tag{5-34}$$

while the maximum steady-state inductor current is found to be

$$I_{L\max} = \frac{V_{out}}{R_{rat}}\left[1 + \frac{R}{2Lf_s}(1 - D_o)\right] = 1.63A. \tag{5-35}$$

The resonant parameters may be estimated once the equations governing the various modes are solved analytically. Fortunately as derived, each mode is governed by a set of linear differential equations, which are readily solved using Laplace transform techniques. In particular, during Mode 2 when the resonant inductor current is increasing up to approximately the minimum of the main inductor current, the following holds:

$$i_r = \frac{V_2}{L_r}t \tag{5-36}$$

To illustrate the sizing of this parameter, mode 2 is assumed to last no longer than 4.8 μsec. It follows from (5-36) that:

$$L_r = \frac{V_2 4.8\mu\,\text{sec}}{I_{L\min}} = .0824mH \tag{5-37}$$

An initial value for capacitor Cr is assumed to be = 260nF. The value is assumed particularly small so that the current stress on S_1 is lessened.

If resonant parameter values L_r = .0824 mH and C_r = 260 nF are not acceptable (as shown by simulation), then the process can be iterated.

E. PSPICE SIMULATION

PSPICE is an interactive circuit simulation program for nonlinear dc, nonlinear transient, and linear AC analyses. Utilizing PSPICE allows the use of predefined semiconductor device models. Figure V-9 illustrates the Prado topology modeled in PSPICE with the circuit components previously given.

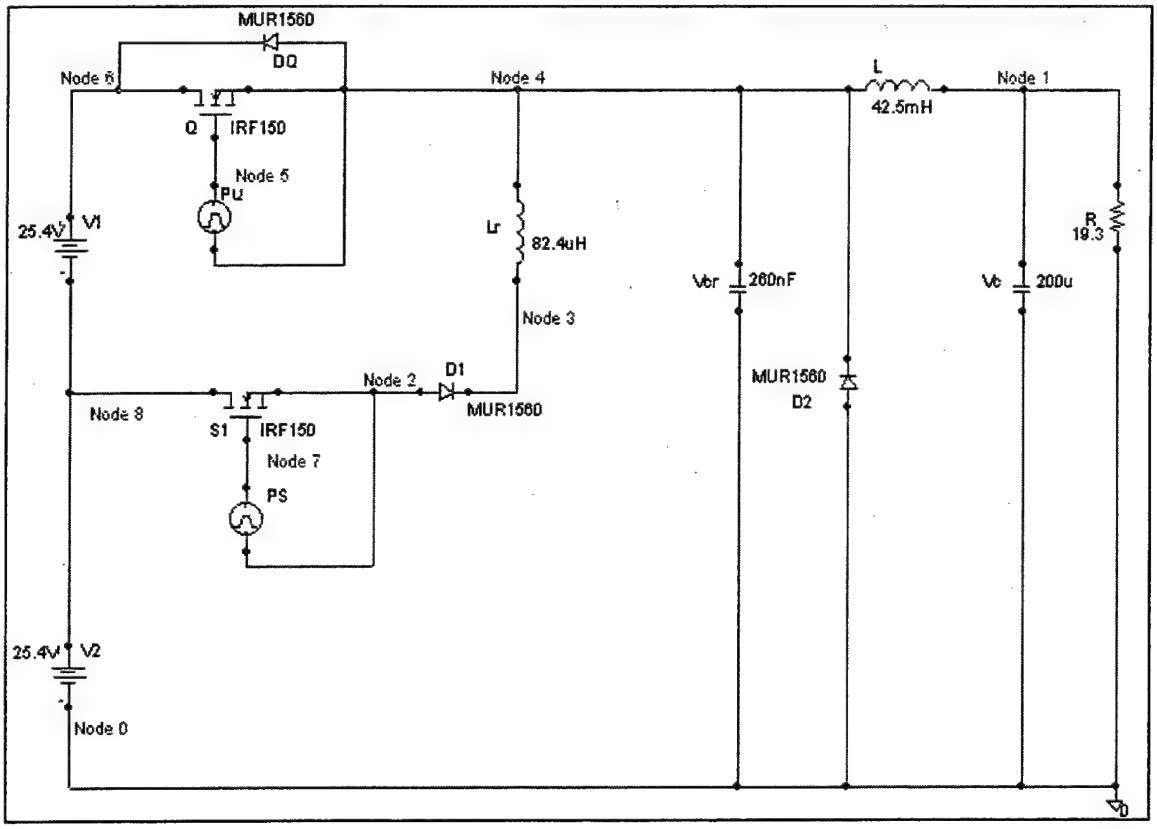

Figure V-9 Prado Topology PSPICE Model

1. Circuit Component Selection

The predetermined circuit component values are C_r = 260 nF, R = 19.3 ohms, L_r = 82.4 uH, and L = 42.5 mH. MUR1560 diodes were selected for their low stored charge

and ultra-fast recovery characteristics. They are frequently used in power switching applications and have a peak repetitive reverse voltage, V_{RRM}, working peak reverse voltage, V_{RWM}, and DC blocking voltage, V_R, of 600V. The diodes can withstand an average rectified forward current, $I_{F(AV)} = 15A$, a peak forward repetitive current, $I_{FRM} = 30A$, and a non-repetitive peak surge current, $I_{FSM} = 200A$. The IRF150 is an n-channel enhancement-mode silicon power field-effect transistor designed for switching applications. With a drain-source voltage, V_{DS}, and drain-gate voltage, V_{DGR}, rated at 100V, and a continuous drain current, $I_D = 40A$ at $T_C = 25^oC$, the transistor is well suited for the circuit.

2. Simulation Evaluation

a) Switch Gating

The switching frequency (f_s) remains fixed at 2kHz. A duty-cycle (D) of 50% is set for the main switch, D_Q, and a duty cycle of 20% is set for the auxiliary switch, D_{S1}. The gating signals used in this model are shown in Figure V-10. Ten-volt square wave pulses are used to gate the IRF150 transistors and their amplitudes are shown here by taking the difference in the node voltages across each pulse generator.

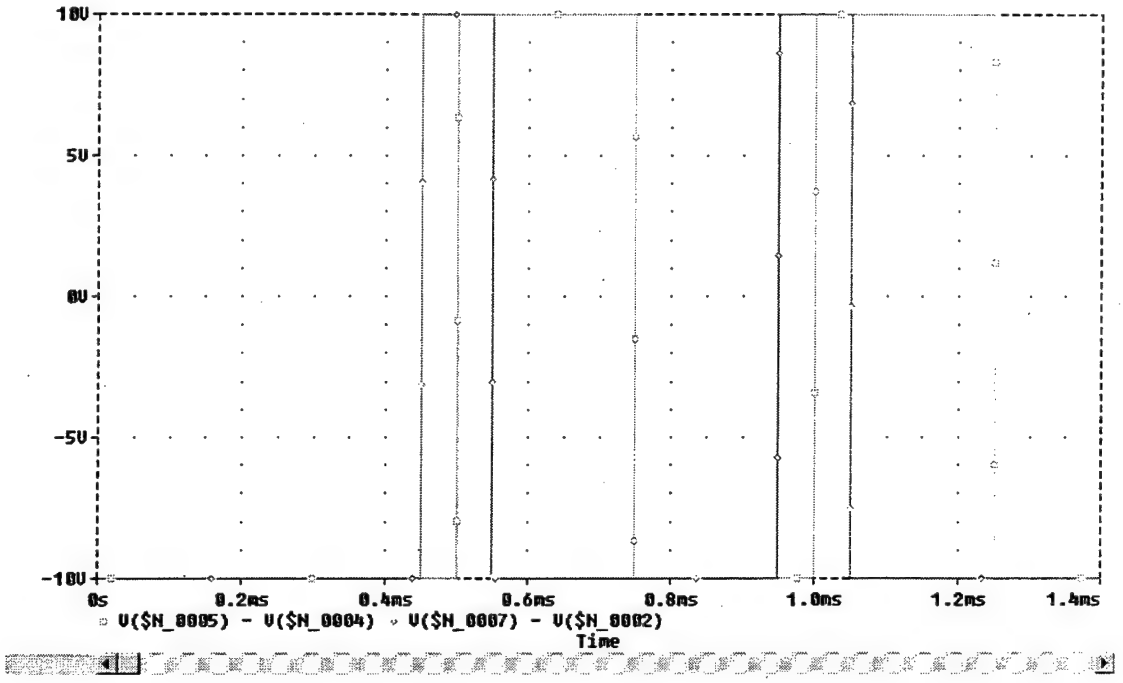

Figure V-10 Switching Frequency

The auxiliary switch, S_1, is the first switch gated which places the circuit into Mode 2. An initial S_1 gate pulse is delayed (t_{DSa}) for 0.45 msec. The auxiliary switch pulse width (PW_{S1}) is as shown in (5-39). The period (T) is found from (5-38).

$$T = \frac{1}{f_s} = 0.5m\sec \tag{5-38}$$

$$PW_{S1} = D_{S1}T = 0.1m\sec \tag{5-39}$$

The auxiliary switch, S_1, closes every 0.5msec (from (5-38)); therefore, S_1 closes at 0.45, 0.95, 1.45, 1.95, 2.45, 2.95ms… and opens at 0.55, 1.05, 1.55, 2.05, 2.55, 3.05ms…

The main switch, Q, is closed at the end of Mode 3, which is the beginning of Mode 4. The initial Q gate pulse is delayed (t_{DQ}) for 0.5msec. The main switch pulse width (PW_Q) is shown below in (5-40).

$$PW_Q = D_Q T = 0.25m\,\text{sec} \tag{5-40}$$

The main switch, Q, closes every 0.5msec; therefore, Q closes at 0.5, 1.0, 1.5, 2.0, 2.5, 3.0ms… and opens at 0.75, 1.25, 1.75, 2.25, 2.75, 3.25ms…

The voltage across the load is depicted in Figure V-11. The voltage levels out at approximately 28V at 40ms.

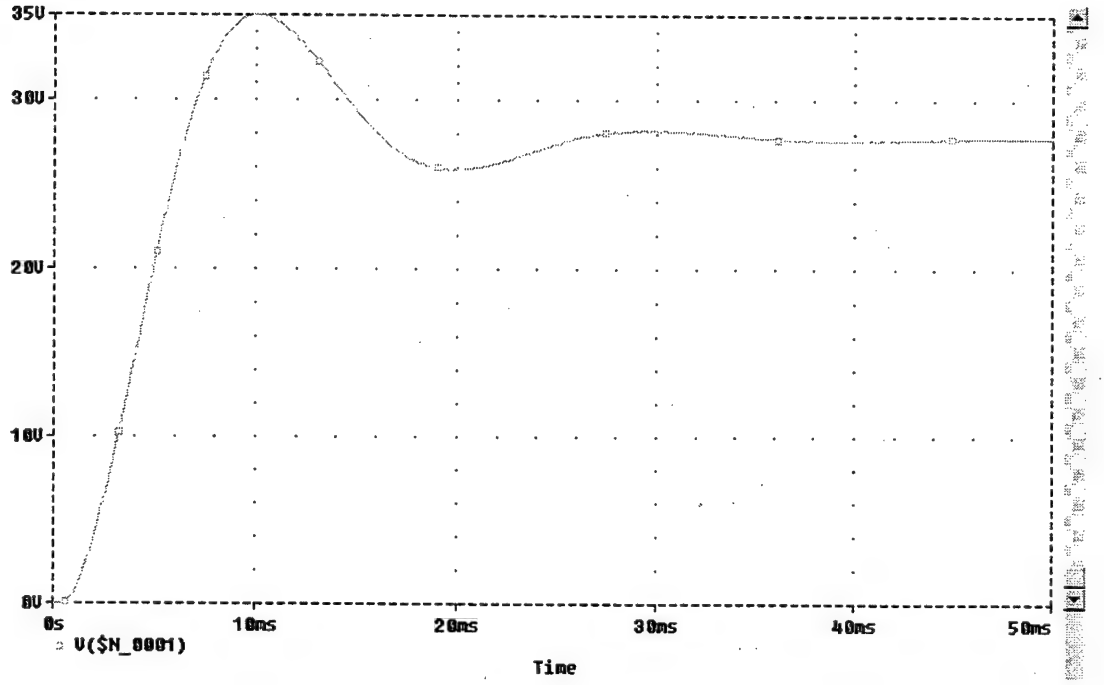

Figure V-11 Load Voltage

b) Switch Performance

The auxiliary switch closes at 49.45ms as shown by the line in Figure V-12. The voltage across S_1 is at a maximum value, but the current through (S_1) demonstrates soft-current switching in the same figure. S_1 turns on softly due to the gradual increase in current through the switch. From Figure V-12, the rise and fall of S_1

current is clearly depicted. This rise and fall is characteristic of the resonance between C_r and L_r in Mode 3. The resonating current across S_1 will improve the switching efficiency of the auxiliary switch as discussed later.

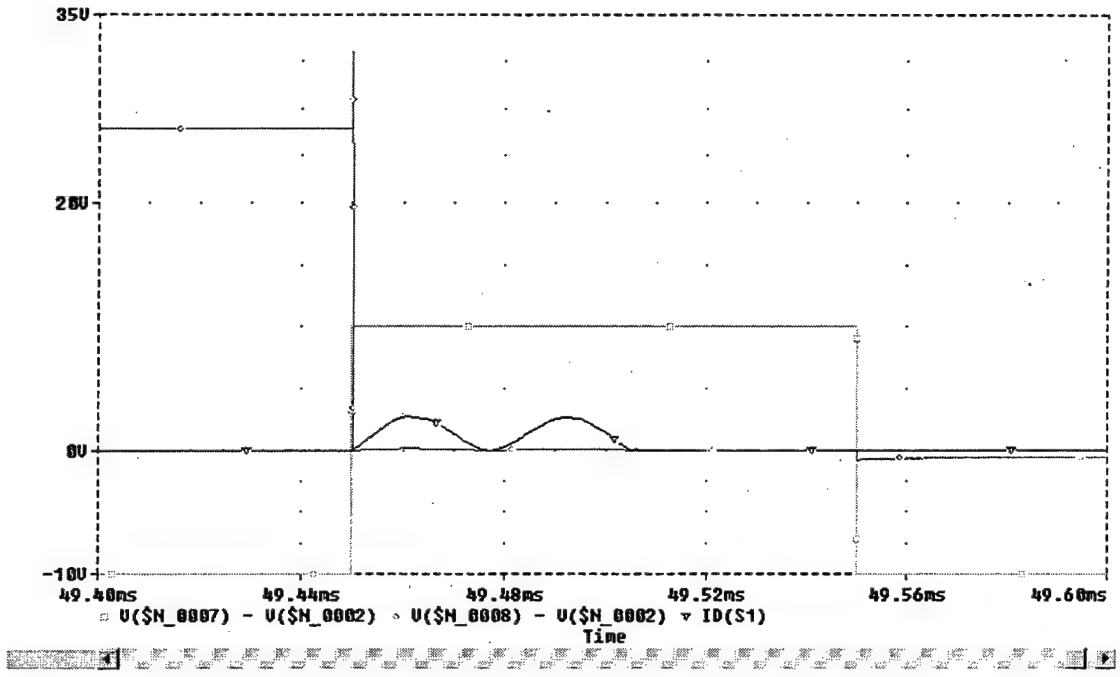

Figure V-12 Auxiliary Switch Characteristics

The main switch closes at 49.5ms as shown by the '0' marked line in Figure V-13. Zero-voltage-switching (ZVS) is realized across Q as seen in the same figure. The voltage across the main switch reaches zero in a cyclic fashion caused by the small value of Cr. The use of this small value of C_r forces great care to be taken in the choice of switching times.

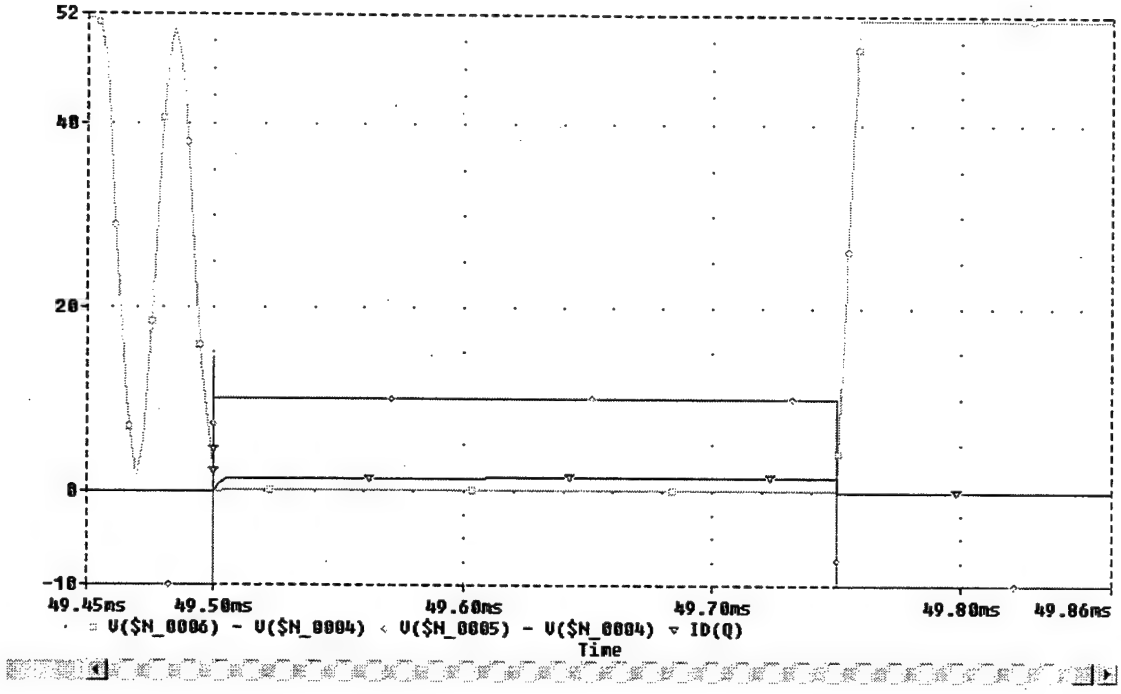

Figure V-13 Main Switch Characteristics

c) Circuit Efficiency

The efficiency of the circuit is easily obtained by dividing the output power by the input power. An efficiency of 95.0% at 180ms and 95.3% at time equal to 200ms is illustrated in Figure V-14. The efficiency levels off to a value of ≅ 95.5% well after the start-up transient is complete.

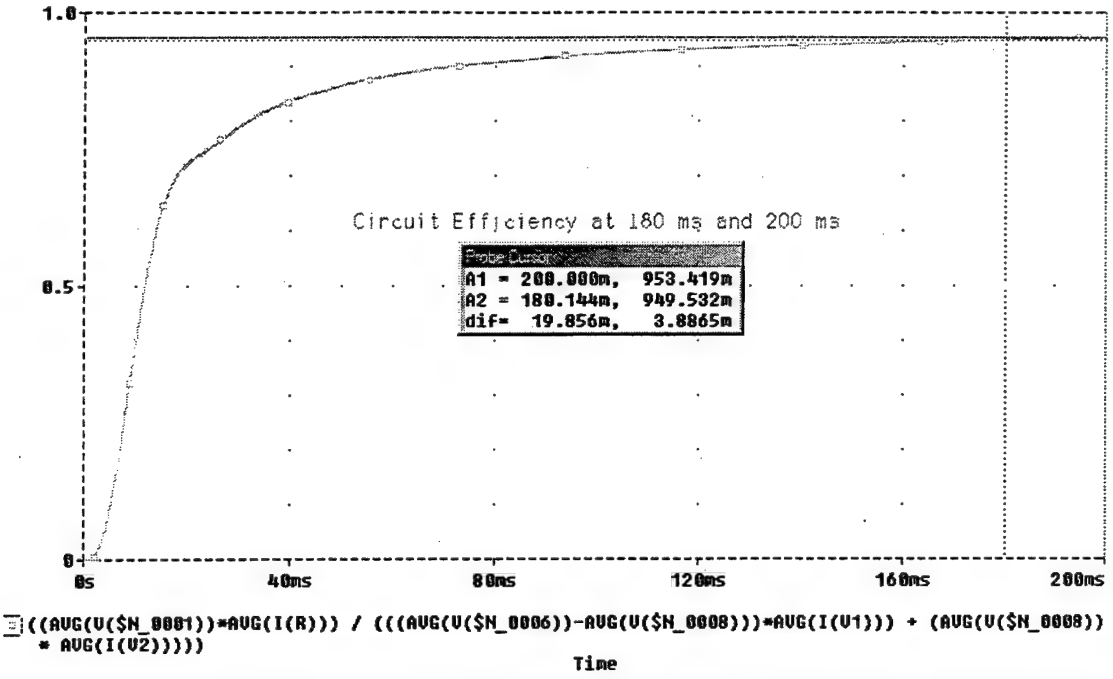

Figure V-14 Circuit Efficiency

Figure V-15 illustrates the Prado topology modeled in PSPICE with the circuit components previously chosen with the exception of the resonant capacitor, C_r. The circuit will now be modeled with C_r = 3uF in order to describe the decrease in efficiency with the use of a larger resonant capacitor. The larger resonant capacitor provides smoother main switch voltage V_Q transitions, which are described later.

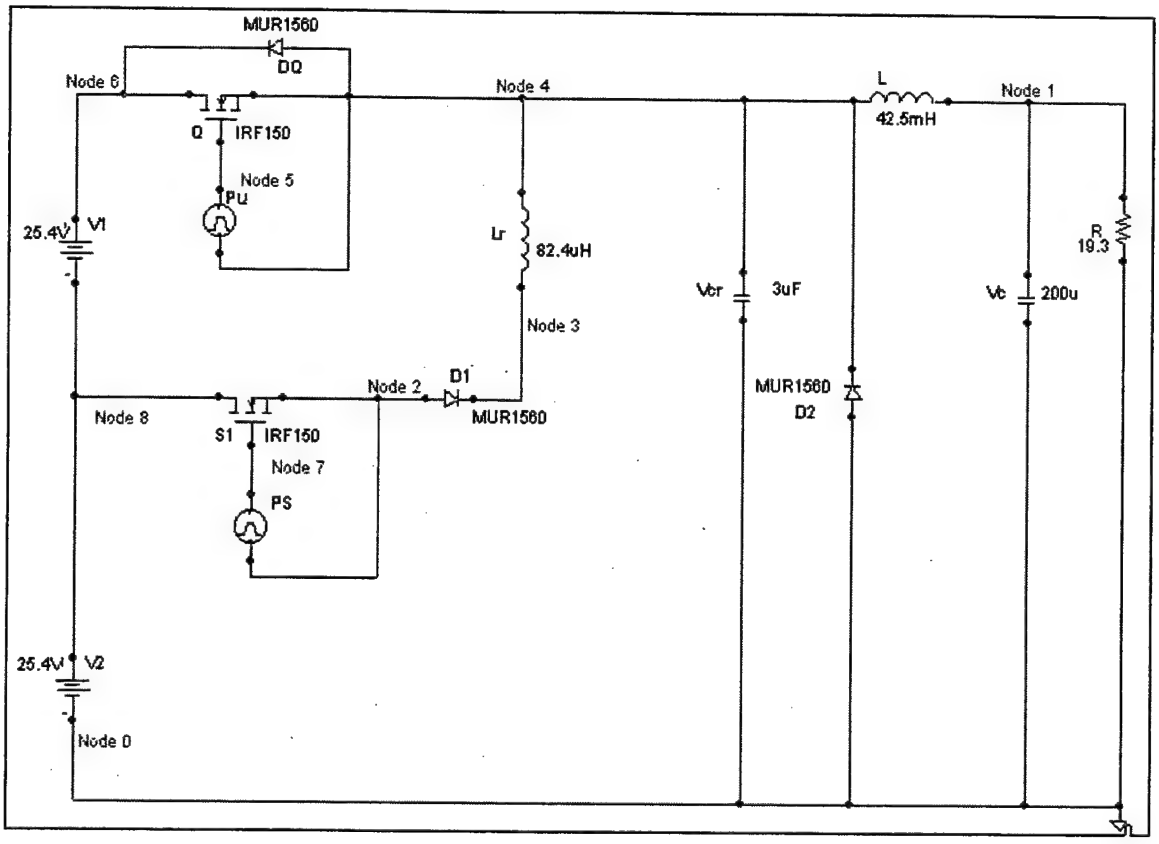

Figure V-15 Prado Topology PSPICE Model with Cr = 3uF

3. Circuit Component Selection Refined

The predetermined circuit component values R = 19.3 ohms, L_r = .165 mH, and L = 42.5 mH remain the same as assigned previously. The sole change to the circuit is the value of the resonant capacitor, C_r = 3.0 uF.

4. Simulation Evaluation Refined

a) Switch Gating

The switching frequency (f_s) remains fixed at 2kHz which is the value from the parameter design section. A duty cycle (D) of 50% is set for the main switch, D_Q, and a duty cycle of 20% is set for the auxiliary switch, D_{S1}. The gating signals used in this model are shown in Figure V-16. Ten-volt square wave pulses are used to gate the IRF150 transistors and their amplitudes are shown by taking the difference in the node voltages across each pulse generator as before.

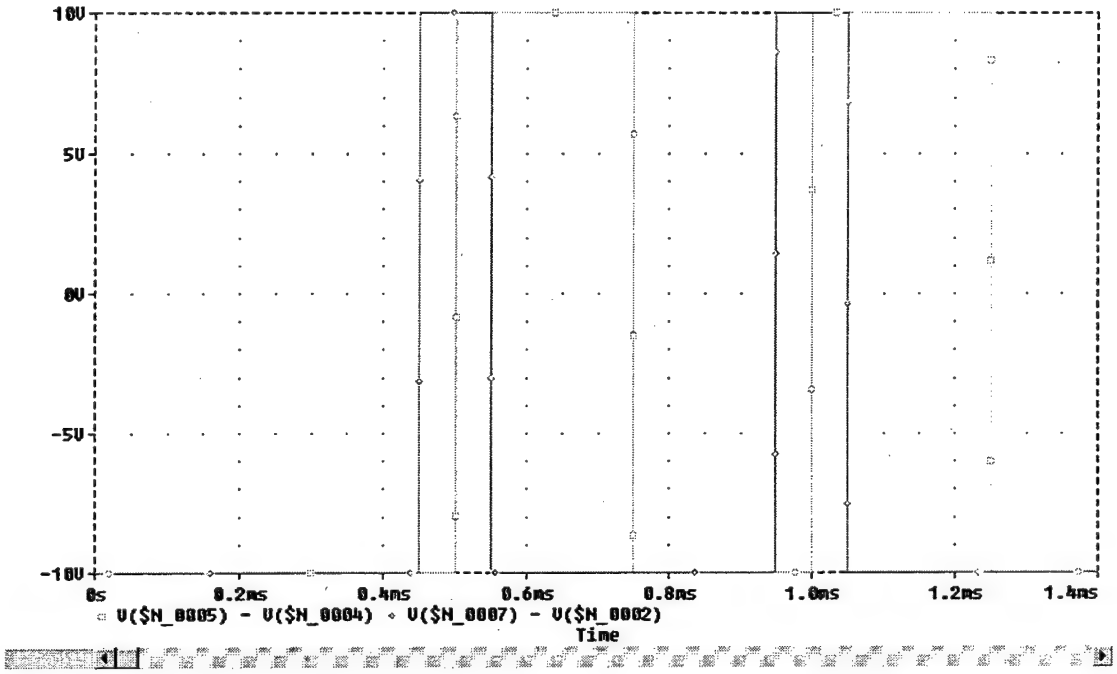

Figure V-16 Switching Frequency

The auxiliary switch, S_1, is again the first switch gated and when gated places the circuit into Mode 2. An initial S_1 gate pulse is delayed (t_{DS1}) for 0.45 msec. The delay is established by setting the PSPICE auxiliary switch pulse generator (PS)

delay parameter. Equation (5-41) gives the auxiliary switch pulse width (PW_{S1}). The period (T) is found from (5-40).

$$T = \frac{1}{f_s} = 0.5m\sec \tag{5-40}$$

$$PW_{S1} = D_{S1}T = 0.1m\sec \tag{5-41}$$

The auxiliary switch, S_1, closes every 0.5msec (from (5-40)); therefore, S_1 closes at 0.45, 0.95, 1.45, 1.95, 2.45, 2.95ms... and opens at 0.55, 1.05, 1.55, 2.05, 2.55, 3.05ms...

The main switch, Q, is closed at the end of Mode 3, which initiates Mode 4. The initial Q gate pulse is delayed (t_{DQ}) for 0.5msec. Calculation of the main switch pulse width (PW_Q) is shown in (5-42).

$$PW_Q = D_Q T = 0.25m\sec \tag{5-42}$$

The main switch, Q, closes every 0.5msec; therefore, Q closes at 0.5, 1.0, 1.5, 2.0, 2.5, 3.0ms... and opens at 0.75, 1.25, 1.75, 2.25, 2.75, 3.25ms...

The voltage across the load is depicted in Figure V-17. The output voltage stabilizes at approximately 28V at 40ms as in the previous circuit.

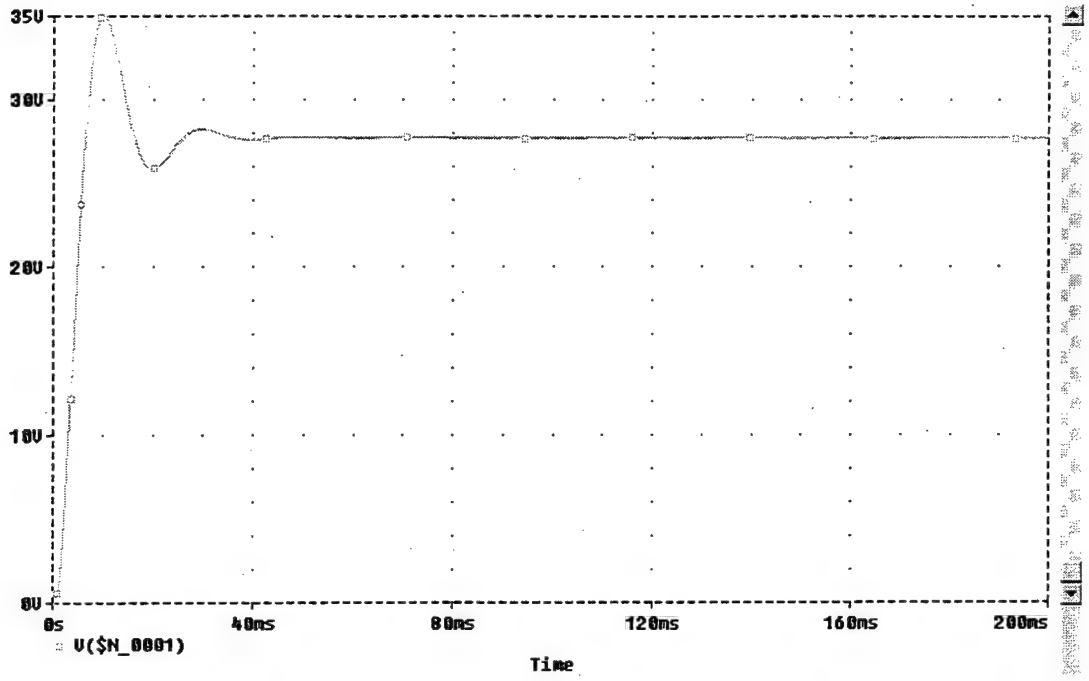

Figure V-17 Load Voltage

b) Switch Performance

The auxiliary switch closes at 49.45ms as shown in the line in Figure V-18. The voltage across S_1 is at a maximum value, but current through (S_1) demonstrates soft-current switching in the same figure. S_1 turns on softly due to the gradual increase in current through the switch. From Figure V-18 the single rise of S_1 current is illustrated. The rise comes without the rapid fall associated with Figure V-12. The average current through (S_1) is larger than the auxiliary switch current seen earlier because C_r is smaller. Because the current is larger, the auxiliary switching losses have increased.

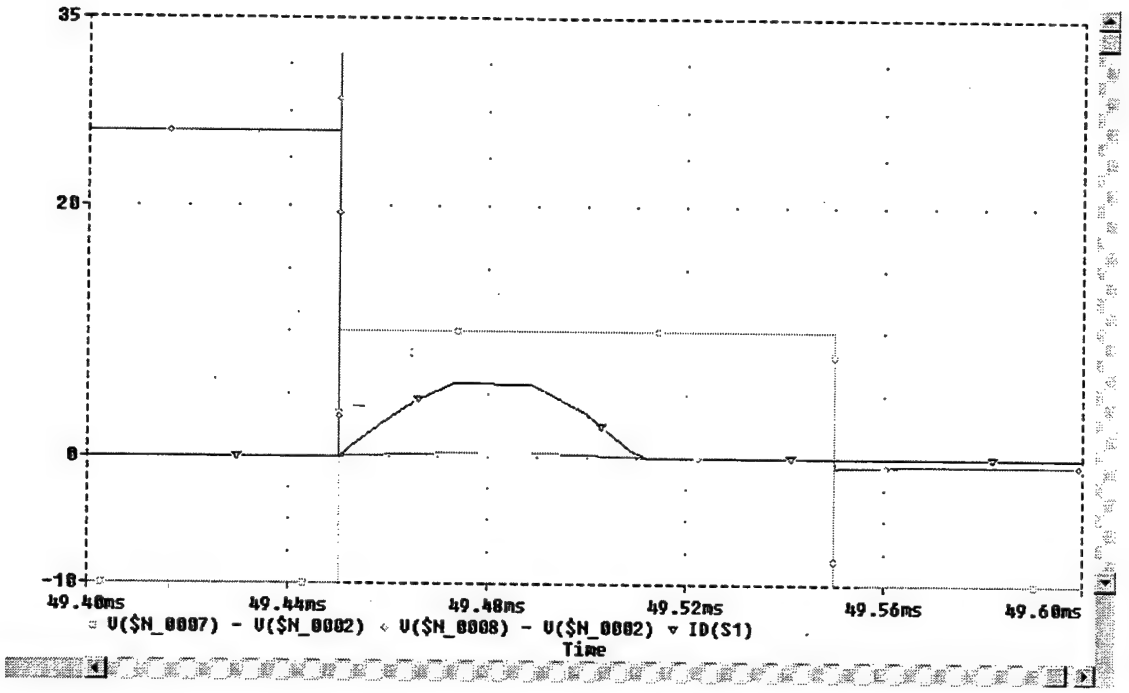

Figure V-18 Auxiliary Switch Characteristics Refined

The main switch closes at 49.5ms as shown by the line in Figure V-19. Zero-voltage switching (ZVS) is realized across Q as seen in the same figure. The voltage across the main switch reaches zero in a smooth linear fashion caused by the large value of C_r. The use of this large value of C_r forces the voltage potential across the main switch, V_Q, to reach approximately zero and remain zero until the main switch is closed.

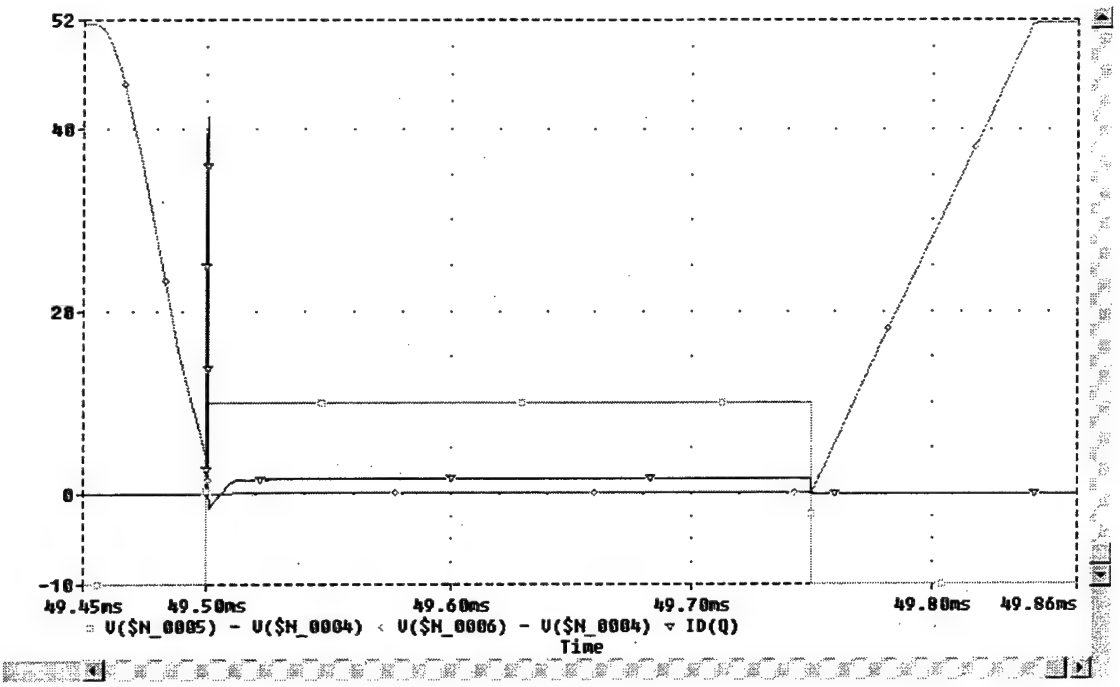

Figure V-19 Main Switch Characteristics Refined

c) Circuit Efficiency Refined

The efficiency of the refined circuit (C_r = 3uF) is obtained by dividing the output power by the input power. An efficiency of 94.8% is obtained at time equal to 180ms as illustrated in Figure V-20. Note the decrease in efficiency when compared to the previous simulation utilizing C_r = 260 nF. This circuit behaves similarly for changes in load.

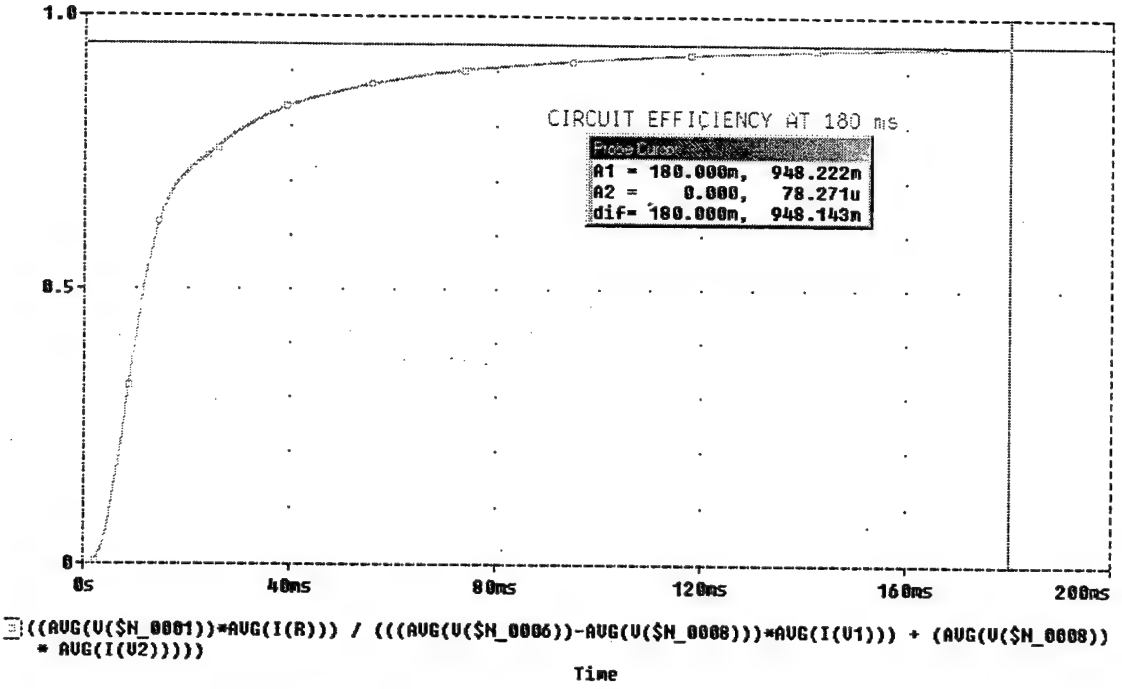

Figure V-20 – Circuit Efficiency Refined

Prado's circuit has been previously defined in this thesis. His topology is not the only two-source approach presented in literature. As an additional reference, the reader is also invited to view a topology created by L.Carlos, D. Ferreira, and V.J. Farias. They presented a paper entitled "A Novel ZCS-ZVS-PWM DC-DC Buck Converter For High Power and High Switching Frequency: Analysis, Simulation and Experimental Results"[5]. It was presented in the IEEE Applied Power Electronics Conference and Exposition in 1993. They achieved soft-switching in much the same way as Prado. The predicted efficiencies are nearly the same as the efficiencies reported for Prado's topology.

Now that several different topologies have been investigated, the documentation in this thesis shifts to the selected topology. The next chapter provides an introduction and analysis of the selected topology for single-source soft switching.

VI. ANALYSIS OF THE SELECTED SINGLE-SOURCE TOPOLOGY

A. INTRODUCTION

The following sections describe the selected soft-switching topology. This topology was chosen because of its possible high-voltage fast-switching applications. The topology is required to meet the SSCM specifications discussed earlier. Because no semiconductor devices are added directly in the buck converter main current path, the maximum efficiency of this circuit is expected to be very high. PSPICE simulations allow an efficiency comparison to be made between this selected converter and the converters described earlier. The principles of operation and the dynamic modeling of the modes for this topology are described in an earlier work [14] and are summarized in the descriptions below.

B. SELECTED TOPOLOGY

G. B. Joung presented a paper in IEEE Power Electronics Specialists Conference, 1996 entitled "New Soft Switched PWM Converter" [12]. In his paper he presented a soft-switching topology which utilized a buck chopper circuit. In this section, Joung's topology and results are discussed. Experimental lab tests, various software simulation studies, and careful theoretical analysis are reported. These evaluations were performed and analyzed in order to find optimum working conditions for the new topology and to enable a better comparison with other novel soft-switching topologies currently available for analysis. In order to accomplish his objective, Joung developed a topology capable of creating zero-voltage and zero-current conditions at the instant of switching. These zero-voltage and zero-current switching conditions allow for major reductions in switching loss and stress.

C. PRINCIPLES OF OPERATION

In order to achieve maximum benefit from Joung's topology, the circuit must be optimized for different circuit input and output voltages. There are optimum component values within the circuit which achieve the desired soft-switching effects capable of being delivered by the topology. Figure VI-1 depicts Joung's overall circuit configuration. The main objective of Joung's topology is to establish a buck chopper circuit that operates at high switching frequencies with minimum switching losses and stresses associated with conventional hard-switching methods.

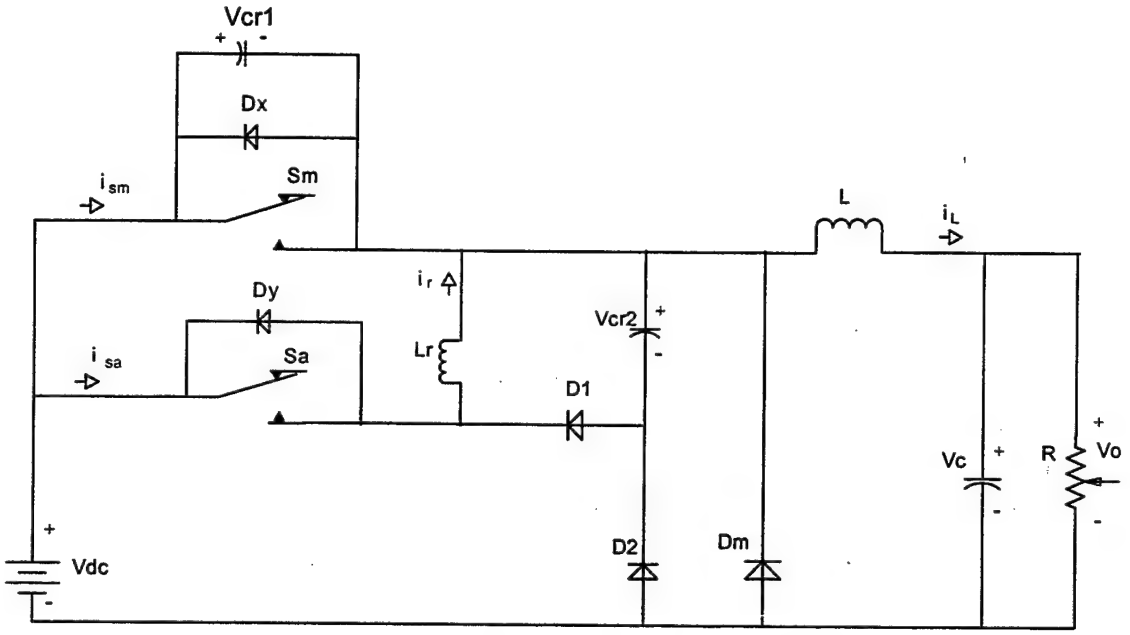

Figure VI-1 - Overall Circuit Configuration

Circuit operation is best described by examining one steady-state switching cycle, which is comprised of eight modes. Each mode describes the principal circuit path in which current flows in the overall topology. Mode transitions flow consecutively for a properly designed circuit. Continuous current conduction mode is assumed. Extensions to discontinuous current conduction are not addressed in this thesis.

The first mode of operation (Mode 1) is illustrated below in Figure IV-2. The main and auxiliary switches are open, the inductor current, i_L, is being transferred to the load, and the main diode, D_m, is conducting. The output capacitor voltage, V_c, is at a steady-state regulated value, $V_c = (D)V_{dc}$, where D is the duty cycle. Capacitor C_{r1} is charged to the input dc voltage, $V_{cr1} = V_{dc}$, capacitor C_{r2} is completely discharged, $V_{cr2} = 0$ V, and there is no current flowing in the resonant inductor, L_r ($i_r = 0$ A). During this mode the inductor current, i_L, will decrease at a constant rate from $i_{L\,max}$ to i_{Lmin}. The main inductor, L, minimum current, i_{Lmin}, occurs at the instant before auxiliary switch, S_a, is closed and Mode 2 begins. The time frame for Mode 1 is measured by the amount of time both switches remain open simultaneously which is controlled by the duty cycles of the main and auxiliary switches.

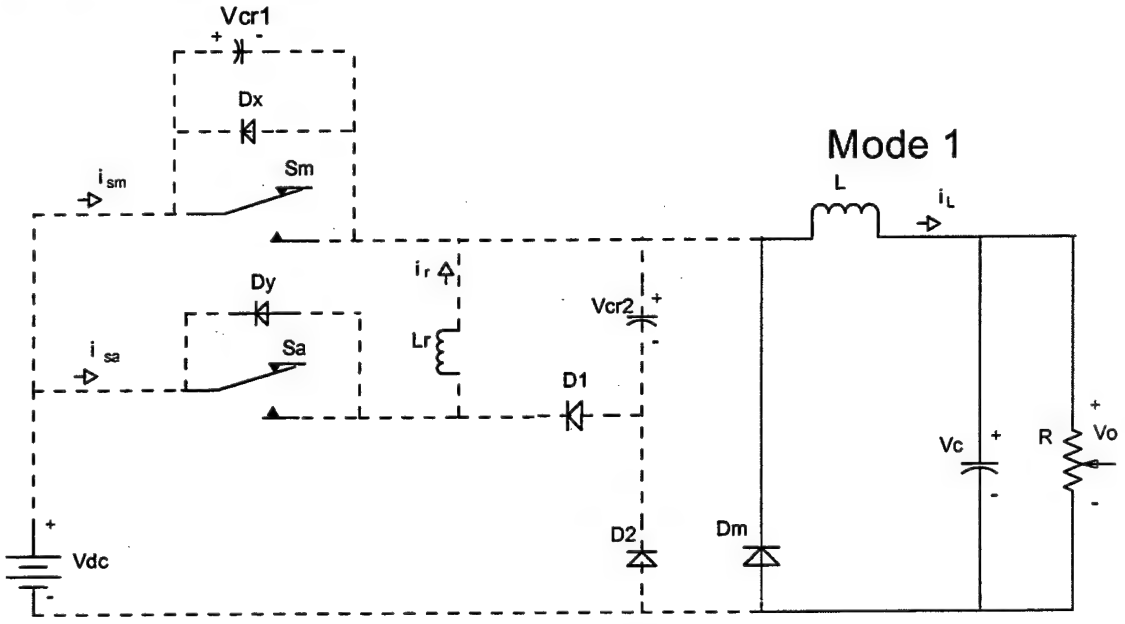

Figure VI-2 – Mode 1

The second mode of operation (Mode 2) begins when the auxiliary switch, S_a, is closed as illustrated in Figure VI-3. Under this condition S_a is closed with a potential of V_{dc} across it, since $V_{cr1} = V_{dc}$. This is a source of switching stress and losses. However, the auxiliary switch current, i_{sa}, is zero and with a properly rated switch, this is a normal

everyday expected switching condition that average market switches can handle with ease. Because i_{sa} increases gradually at a rate equal to the rate of change in i_r, given by $\frac{d}{dt} i_r = \frac{V_{dc}}{L_r}$, the switching is referred to as soft switching under zero-current conditions.

Initially as S_a is closed, D_m is still conducting. This condition places the source voltage, V_{dc}, across L_r, therefore $V_{Lr} \cong V_{dc}$. Since $\frac{d}{dt} i_r = \frac{V_{dc}}{L_r}$, the resonant inductor current, i_r, increases rapidly until $i_r = i_L$ (where i_L is still quite close to I_{Lmin}), provided V_{dc} is large when compaired to L_r. This condition starves the main diode D_m of current causing it to naturally turn off. Because D_m is now off, the negative side of C_{r1} is no longer common to the negative potential of V_{dc} and thus C_{r1} is no longer in parallel with V_{dc}. Therefore, V_{cr1} is free to vary as dictated by the newly created resonant circuit.

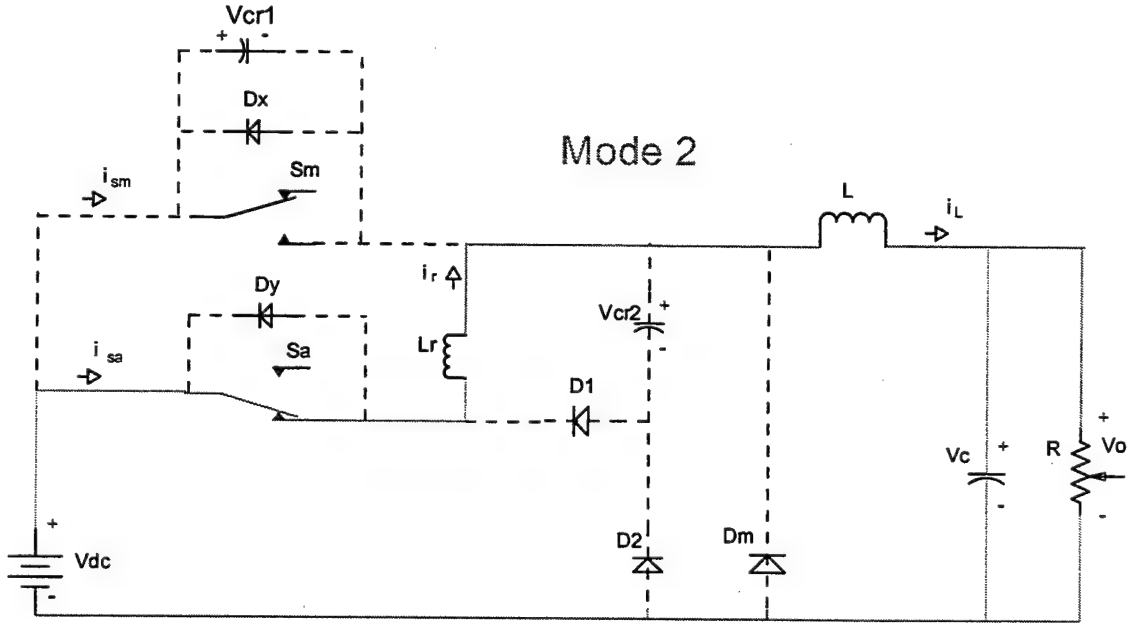

Figure VI-3 – Mode 2

In the third mode (Mode 3), the resonant condition created at the end of the second mode is seen in Figure VI-4. Initialy $i_r = i_L$ and $V_{cr1} = V_{dc}$. An L_r-C_{r1} loop is created when L is much bigger than L_r as seen in Figure VI-5. This loop causes V_{cr1} to be

driven down to a new equilbrium value, $V_{cr1} = 0$ V. The diode D_x prevents V_{cr1} from resonating past approximately –1V. At this point, a near zero-voltage condition has been created across the main switch, S_m. Mode 3 ends when S_m is closed.

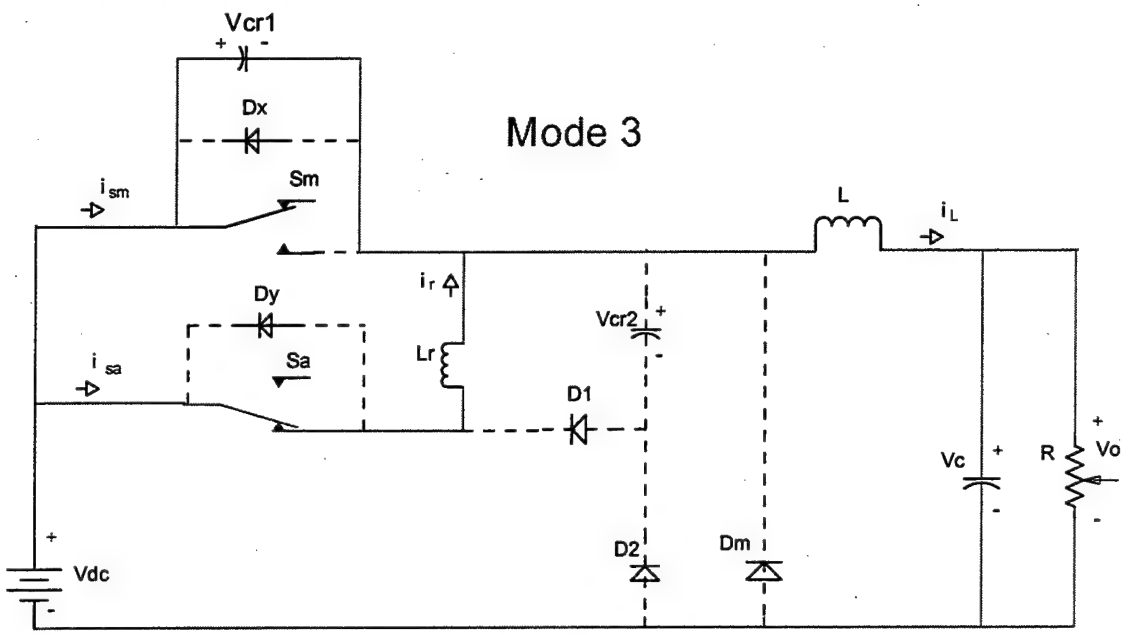

Figure VI-4 – Mode 3

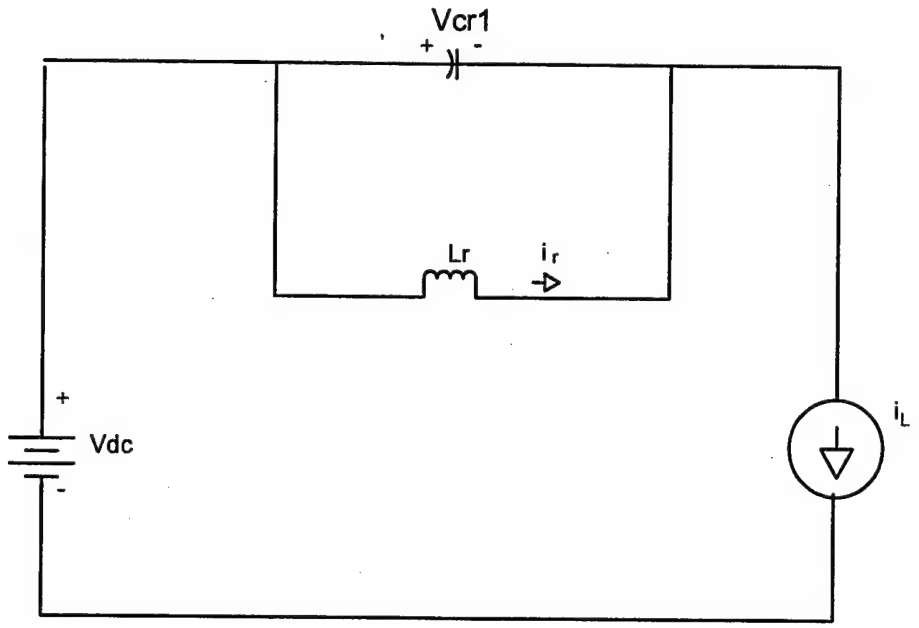

Figure VI-5 – Mode 3 Approximation

The fourth mode (Mode 4) begins when the main switch, S_m, is closed with V_{cr1} at approximately zero volts, therefore zero-voltage switching is realized across the main switch. With S_m closed, V_{cr1} is clamped at near zero volts. Because L_r is effectively in parallel with the conducting main switch, the voltage across L_r is approximately zero, so i_r is held constant. Since i_r is constant, the main switch current, i_{Sm}, tracks the linear increase in current through the main inductor, i_L. The available current paths are depicted in Figure VI-6. The voltage drop across the closed auxiliary switch, S_a, is approximately zero, auxiliary switch S_a may now be opened.

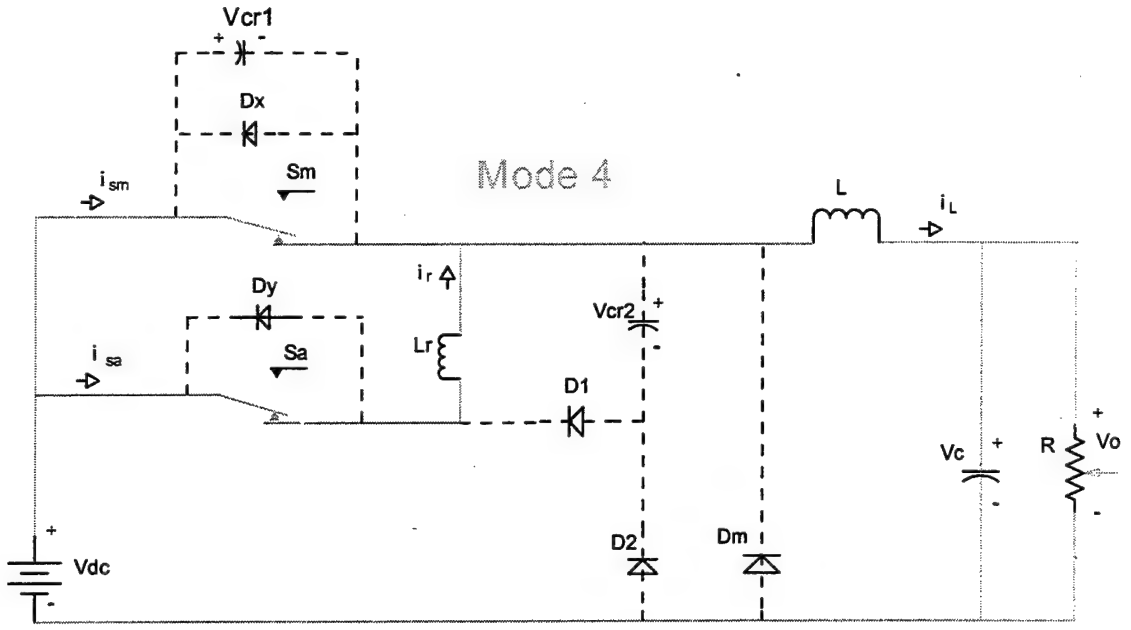

Figure VI-6 - Mode 4

The fifth mode (Mode 5) begins the instant the auxiliary switch is opened. At the instant S_a is opened, the circuit current flow exists as illustrated in Figure VI-7. As shown in Figure VI-7 the resonant inductor current, i_r, must continue to flow, therefore diode D_1 turns on and the previously uncharged C_{r2} begins to charge. The resonant loop formed by L_r and C_{r2} drives i_r to zero, then diode D_1 is current starved and C_{r2} stops charging. With S_a open, the main switch current, i_{Sm}, equalizes with i_L.

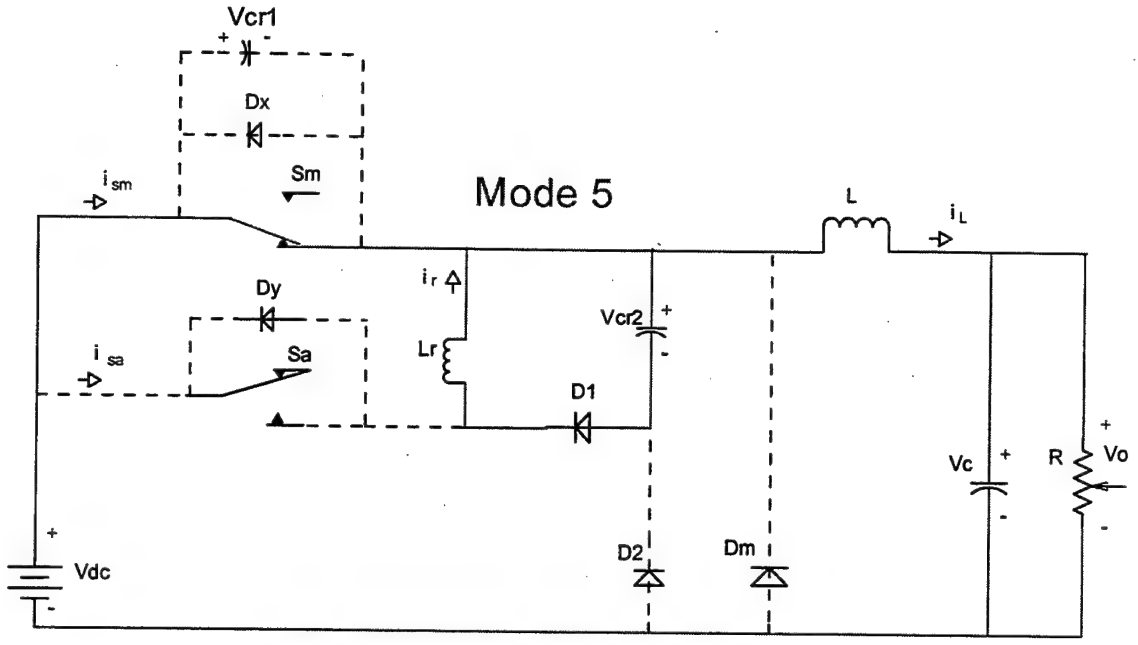

Figure VI-7 - Mode 5

There is an extension to Mode 5 when the following condition exists. The new mode, Mode 5x, is depicted in Figure VI-8. This mode exists if the voltage across charging resonant capacitor two, Vcr2, attempts to exceed V_{dc}. If Vcr2 attempts to exceed V_{dc}, diode D_2 becomes forward biased and creates the "new" decay path illustrated in Figure VI-8. Since $\frac{d}{dt} i_r = \frac{-V_{dc}}{L_r}$, i_r quickly decays to zero, diodes D_1 and D_2 are naturally turned off, while V_{cr2} is frozen at approximately V_{dc}.

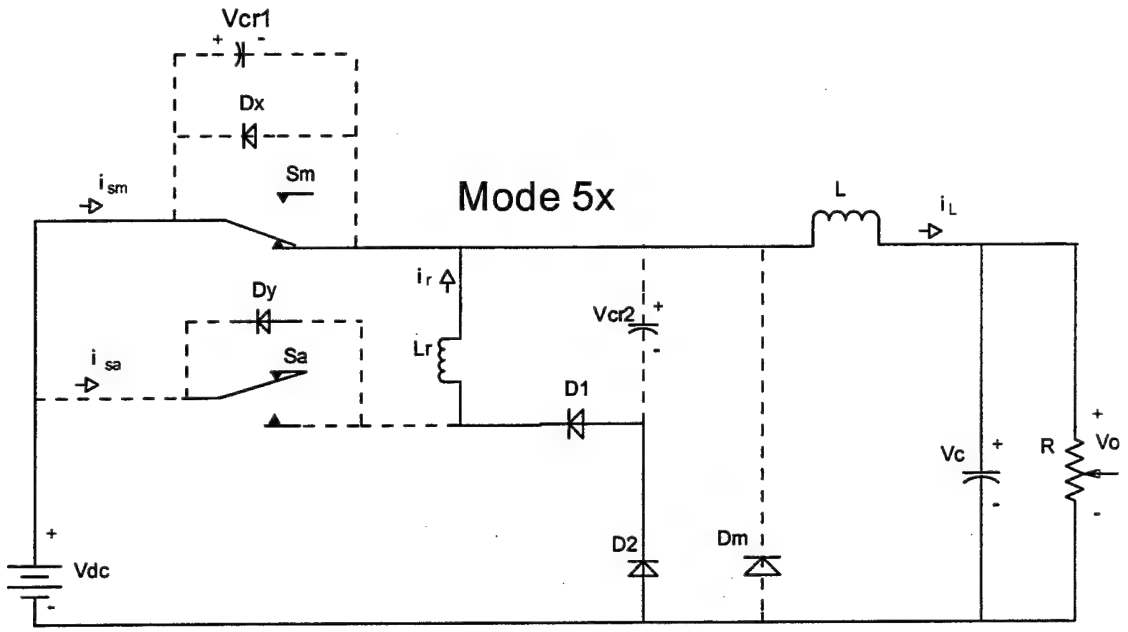

Figure VI-8 - Mode 5x

The sixth mode (Mode 6) exists during the interval of time in which the main switch, S_m, carries the full inductor current, i_L, as dictated by the duty-cycle control. The flow of current is illustrated in Figure VI-9. Resonant capacitor two voltage, V_{cr2}, has been charged to some positive voltage between 0V and V_{dc} and the resonant inductor current, i_r, is zero. This mode ends when the main switch, S_m, is opened. The circuit will now enter Mode 7a or Mode 7b depending on the level to which V_{cr2} has been charged. If $V_{cr2} < V_{dc}$, then the operation is described by Mode 7a; otherwise, operation skips to Mode 7b.

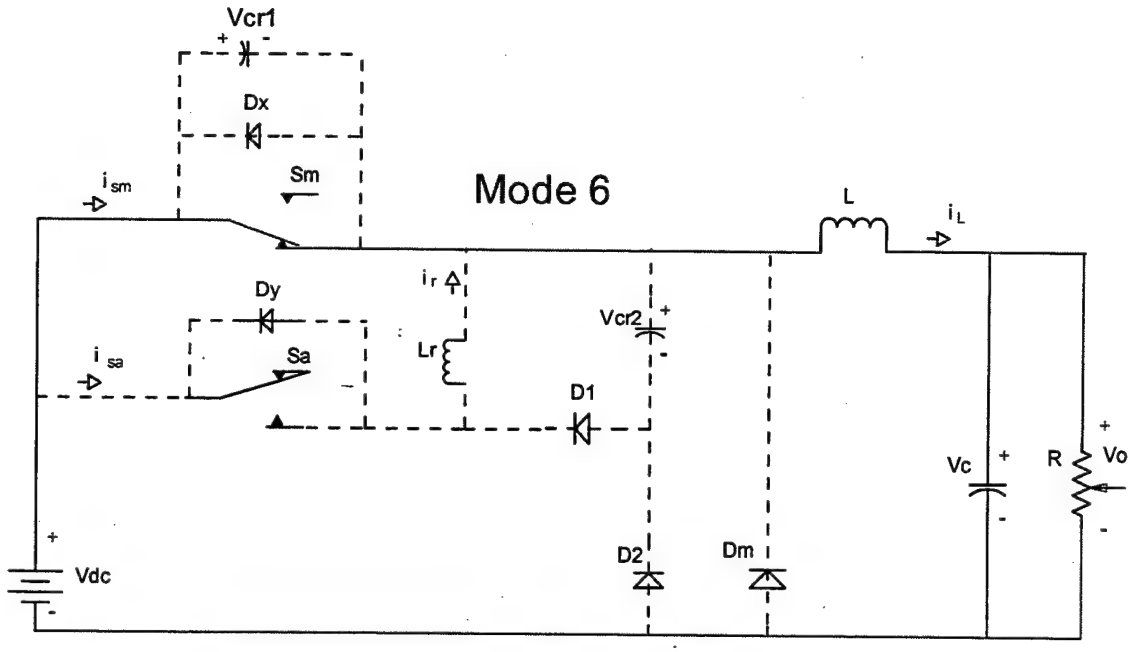

Figure VI-9 - Mode 6

Note, at the end of Mode 3 V_{cr1} is approximately zero volts. When S_m is opened, the current i_L must remain continuous and therefore will flow through C_{r1}. This current path is shown in Figure VI-10. Since $V_{D2} = V_{cr1} + V_{cr2} - V_{dc}$, the charging of C_{r1} will eventually cause V_{D2} to go positive so that D_2 is forward biased and begins to conduct. This causes the circuit to transition to Mode 7b.

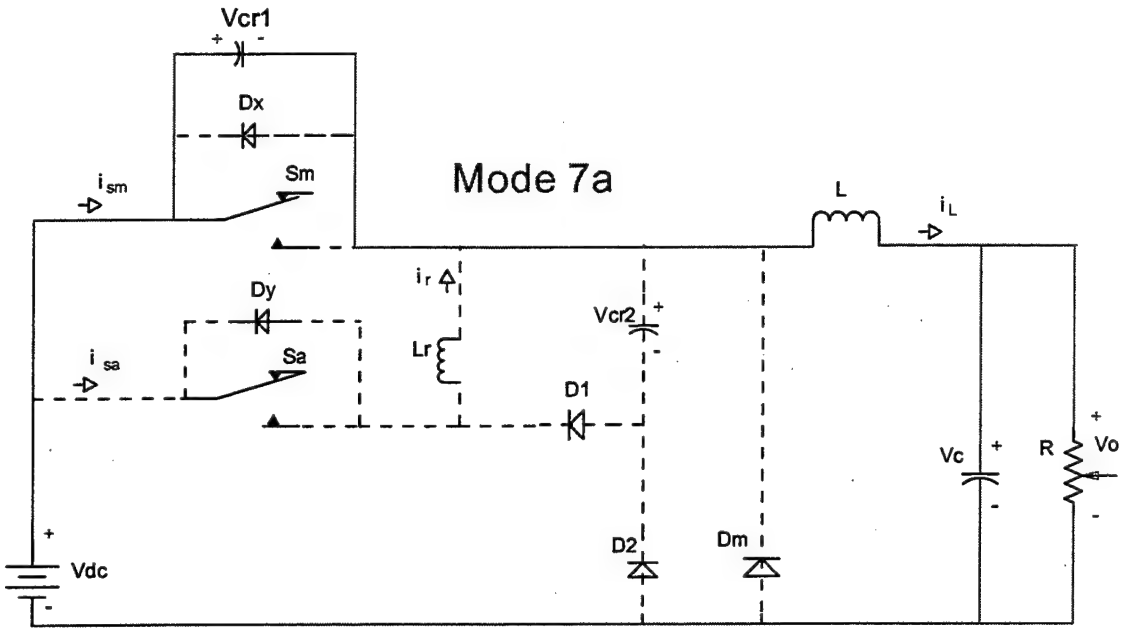

Figure VI-10 - Mode 7a

With $V_{D2} = V_{cr1} + V_{cr2} - V_{dc}$ and C_{r1} charging, D_2 begins conducting and the governing circuit is illustrated in Figure VI-11. Because Kirchhoff's Voltage Law demands that $V_{cr1} + V_{cr2} = V_{dc}$ as C_{r1} is charging, C_{r2} must be discharging. Mode 7b completes when V_{cr1} charges slightly past V_{dc}, V_{cr2} is discharged to approximately zero volts, and D_2 naturally turns off.

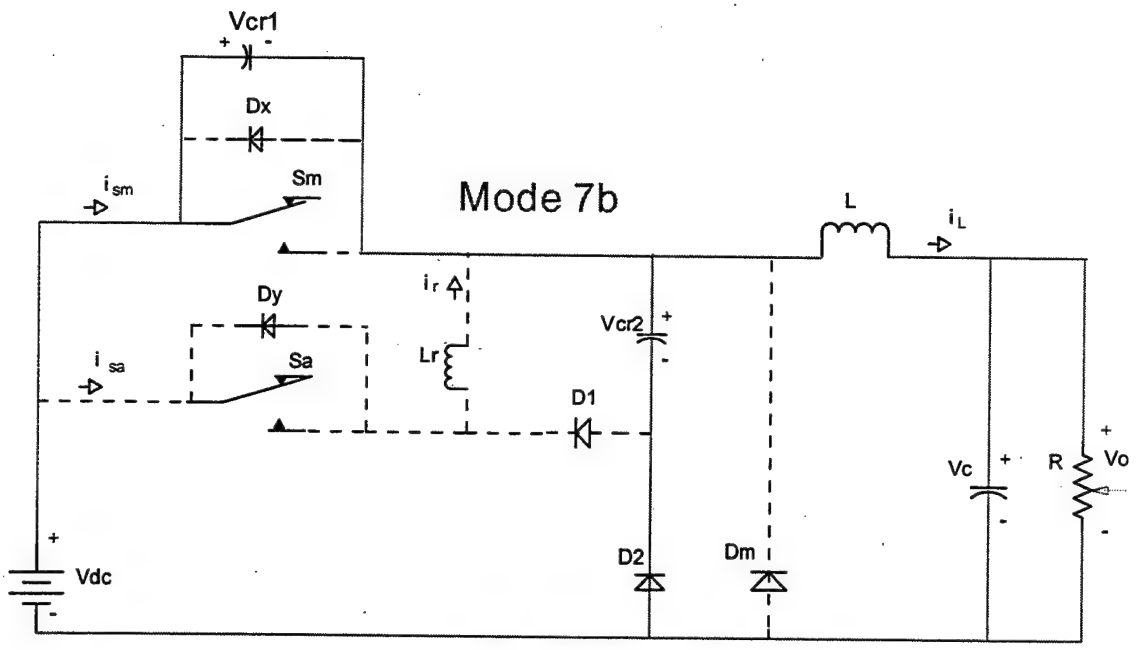

Figure VI-11 - Mode 7b

Mode 1 is re-initiated once V_{cr1} charges slightly beyond V_{dc} and the main diode D_m becomes forward biased since $V_{Dm} = V_{cr1} - V_{dc}$. Based on the fact that $V_{cr1} + V_{cr2} = V_{dc}$, it is clear that C_{r1} is discharged and all of the inductor current, i_L, is transferred to the freewheeling diode, D_m. The current flow is described in Figure VI-12 where Mode 8 is equivalent to Mode 1. The next steady-state switching cycle is now ready to begin as $V_{cr2} = 0V$, $i_r = 0A$, and $V_{cr1} = V_{dc}$.

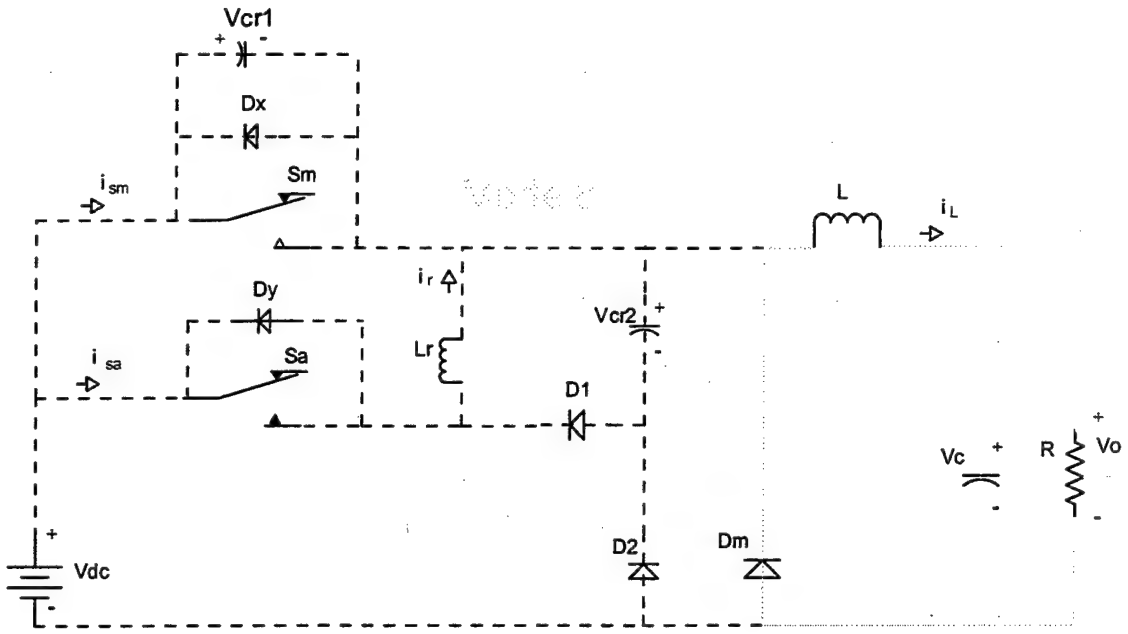

Figure VI-12 - Mode 8

D. MATHEMATICAL MODEL DEVELOPMENT

Each of the eight modes of operation previously described is governed by a set of differential equations prescribed by the circuit configuration. The transitions between modes are specified by conditions on the network state variables. This section documents the state equations for each mode and sets forth each transition constraint.

For the circuit under consideration, the state variables correspond to the currents or voltages of the five energy storage elements. In particular i_L, V_c, V_{cr1}, V_{cr2}, and i_r are the state variables. All equations are derived assuming zero switch and diode conduction drops, ideal inductors and capacitors, and a stiff dc input voltage source. The following equations describe the corresponding dynamics for each mode.

1. Mode 1

The dynamics shown below are derived from the Mode 1 circuit depicted in Figure VI-2.

$$\frac{d}{dt}i_L = -\frac{V_c}{L} \tag{6-1}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{6-2}$$

$$\frac{d}{dt}i_r = 0 \tag{6-3}$$

$$\frac{d}{dt}V_{cr1} = 0 \tag{6-4}$$

$$\frac{d}{dt}V_{cr2} = 0 \tag{6-5}$$

All quantities not changing are held at the values attained at the end of Mode 8. Transition to Mode 2 begins when a gating signal is applied to the auxiliary switch, S_a. The gating signal is synchronized with the clocking signal used to activate the main switch, S_m, described later in Mode 4.

2. Mode 2

The dynamics shown below are derived from the Mode 2 circuit depicted in Figure VI-3.

$$\frac{d}{dt}i_L = -\frac{V_c}{L} \tag{6-6}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{6-7}$$

$$\frac{d}{dt}i_r = \frac{V_{dc}}{L_r} \tag{6-8}$$

$$\frac{d}{dt}V_{cr1} = 0 \tag{6-9}$$

$$\frac{d}{dt}V_{cr2} = 0 \tag{6-10}$$

These equations govern circuit operation up until $i_r = i_L$. Once $i_r = i_L$ the circuit has transitioned into Mode 3.

3. Mode 3

The dynamics shown below are derived from the Mode 3 circuit depicted in Figure V-4.

$$\frac{d}{dt}i_L = \frac{V_{dc} - V_c - V_{cr1}}{L} \tag{6-11}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{6-12}$$

$$\frac{d}{dt}i_r = \frac{V_{cr1}}{L_r} \tag{6-13}$$

$$\frac{d}{dt}V_{cr1} = \frac{i_L - i_r}{C_{r1}} \tag{6-14}$$

$$\frac{d}{dt}V_{cr2} = 0 \tag{6-15}$$

The initial condition on voltage V_{cr1} is approximately V_{dc} as set by a subsequent mode. Also, diode D_x constrains V_{cr1} from going negative. Thus, V_{cr1} must be monitored for this condition in order for the circuit to correctly transition to Mode 4.

4. Mode 4

Mode 4 is initiated when either $V_{cr1} = 0V$ (if that condition is used in the control) or when the main switch is closed as dictated by the duty-cycle control. The dynamics shown below are derived from the Mode 4 circuit depicted in Figure VI-6.

$$\frac{d}{dt} i_L = \frac{V_{dc} - V_c}{L} \tag{6-16}$$

$$\frac{d}{dt} V_c = \frac{1}{C} i_L - \frac{V_c}{RC} \tag{6-17}$$

$$\frac{d}{dt} i_r = 0 \tag{6-18}$$

$$\frac{d}{dt} V_{cr1} = 0 \tag{6-19}$$

$$\frac{d}{dt} V_{cr2} = 0 \tag{6-20}$$

The current through the main switch is given by:

$$i_{Sm} = i_L - i_r \tag{6-21}$$

5. Mode 5

Mode 5 is initiated when auxiliary switch S_a is turned off. The turn off may be specified based on some sensed variable or based simply on a timing criterion (more on this later). The dynamics shown below are derived from the Mode 5 circuit depicted in Figure VI-7.

$$\frac{d}{dt}i_L = \frac{V_{dc} - V_c}{L} \tag{6-22}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{6-23}$$

$$\frac{d}{dt}i_r = -\frac{V_{cr2}}{L_r} \tag{6-24}$$

$$\frac{d}{dt}V_{cr1} = 0 \tag{6-25}$$

$$\frac{d}{dt}V_{cr2} = \frac{i_r}{C_{r2}} \tag{6-26}$$

These dynamics govern up until i_r decays to zero or if V_{cr2} increases up to V_{dc}, then the circuit transitions to Mode 5x.

6. Mode 5x

The dynamics shown below are derived from the Mode 5x circuit depicted in Figure VI-8. If V_{cr2} tries to go above V_{dc} then:

$$\frac{d}{dt}V_{cr2} = 0 \tag{6-27}$$

so that:

$$V_{cr2} = V_{dc} \tag{6-28}$$

Also as shown in the Mode 5x circuit,

$$\frac{d}{dt}i_r = -\frac{V_{dc}}{L_r} \tag{6-29}$$

Mode 5x persists up until the resonant inductor current i_r, goes to zero.

7. Mode 6

Once i_r goes to zero, Mode 6 is entered and the governing equations are found by inspecting the circuit depicted in Figure VI-9.

$$\frac{d}{dt}i_L = \frac{V_{dc} - V_c}{L} \tag{6-30}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{6-31}$$

$$\frac{d}{dt}i_r = 0 \tag{6-32}$$

$$\frac{d}{dt}V_{cr1} = 0 \tag{6-33}$$

$$\frac{d}{dt}V_{cr2} = 0 \tag{6-34}$$

For Mode 6, V_{cr2} is held at some positive value between zero and V_{dc} and i_r is held at zero. These equations hold until the main switch is opened, ending Mode 6.

8. Mode 7a

If $V_{cr1} < V_{dc}$, then the state variable dynamics are given by analysis of the Mode 7a circuit depicted in Figure VI-10.

$$\frac{d}{dt}i_L = \frac{V_{dc} - V_c - V_{cr1}}{L} \tag{6-35}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{6-36}$$

$$\frac{d}{dt}i_r = 0 \tag{6-37}$$

$$\frac{d}{dt}V_{cr1} = \frac{i_L}{C_{r1}} \tag{6-38}$$

$$\frac{d}{dt}V_{cr2} = 0 \tag{6-39}$$

These equations hold up until $V_{cr1} + V_{cr2} = V_{dc}$. At which point, D_2 begins conducting and the circuit transitions to Mode 7b.

9. Mode 7b

The dynamics shown below are derived from the Mode 7b circuit depicted in Figure VI-11.

$$\frac{d}{dt}i_L = \frac{V_{cr2} - V_c}{L} \tag{6-40}$$

$$\frac{d}{dt}V_c = \frac{1}{C}i_L - \frac{V_c}{RC} \tag{6-41}$$

$$\frac{d}{dt}V_{cr1} = \frac{i_L}{C_{r1} + C_{r2}} \tag{6-42}$$

$$\frac{d}{dt}i_r = 0 \tag{6-43}$$

Since V_{cr2} is algebraically related to state variable V_{cr1} and input V_{dc} as shown in the Mode 7b circuit depicted in Figure VI-11, it is constrained by:

$$V_{cr2} = V_{dc} - V_{cr1} \tag{6-44}$$

These equations govern operation up until $V_{cr1} = V_{dc}$. That transition condition then moves operation back to Mode 1.

This section has set forth the dynamic equations for the individual modes together with the transition conditions. The next section utilizes the equations derived here and PSPICE simulation to model the Joung topology with selected circuit specifications. In a later section the PSPICE model will be compared to lab results.

E. SPECIFICATIONS AND COMPONENT SELECTION

For the given topology under construction, the design engineer must select five component values: the main inductance, L, the main output capacitance, C, the resonant inductance, L_r, and the two resonant capacitances, C_{r1} and C_{r2}. In addition the designer must specify the switching frequency and establish the criteria for turning the auxiliary switch S_a off. A control algorithm must be formulated and suitably fast diodes selected

for the network. One nuance that has thus far been overlooked is the presence of C_{r1} directly across the main switch S_m. If there is any charge on C_{r1} when S_m is closed, the switch will be destroyed. Therefore, it is probably more proper to think of this capacitance as internal to the switch itself. For this section and in order to gain an appreciation for the dependence of the parameter values on the circuit operation, it is assumed that C_{r1} is a passive component that will be selected.

The basic design of a buck chopper is well understood and will be briefly highlighted next. For convenience and later lab modeling, the following specifications are assumed: the input voltage V_{dc} is fixed at 50.8V, the desired output voltage is 30V, the rated output load is 46.6W, the switching frequency is set at 2kHz, and the output ripple should be less than 0.1V. The main inductor is sized principally to ensure that the converter remains in the continuous current conduction mode for all loads greater than 10% of rated (R_{rat} = 19.31 Ω). With the nominal duty-cycle given by

$$D_o = \frac{30V}{50.8V} = 0.5906 \tag{6-45}$$

the load resistance at 10% power is given by

$$R_{crit} = 10R_{rat} = 193.1\Omega, \tag{6-46}$$

the critical inductance is found to be:

$$L_{crit} = \frac{R_{crit}}{2f_s}(1 - D_o) = 19.8mH. \tag{6-47}$$

Here 'f_s' is the switching frequency in Hz. In order to ensure continuous conduction mode, L is fixed at 42.5mH. Next, the minimum capacitance is estimated from the following steady-state ripple constraint:

$$C_{\min} = \frac{D_o}{8Lf_s^2\Delta V_{out}}(V_{dc} - V_{out}) = 90.3\mu F \tag{6-48}$$

Here V_{out} is the assumed peak-to-peak output ripple of 0.1V. The actual selection of the capacitor is strongly influenced by the control loop design. If C is selected too small then there is insufficient energy in the capacitor to maintain the output voltage during a transient. If C is selected too large then a small variation in the output voltage will result

in the duty cycle bouncing between full-on and full-off. This occurs because there is too much energy in the capacitor compared to what the inductor can handle. In this case, it is postulated that C = 200μF yields a good compromise between available energy for transients and dynamic range in the control loop.

For rated load, it is also of interest to quantify the expected ripple current. The minimum steady-state inductor current is found to be:

$$I_{L\min} = \frac{V_{out}}{R_{rat}}\left[1 - \frac{R}{2Lf_s}(1 - D_o)\right] = 1.48A \tag{6-49}$$

while the maximum steady-state inductor current is found to be:

$$I_{L\max} = \frac{V_{out}}{R_{rat}}\left[1 + \frac{R}{2Lf_s}(1 - D_o)\right] = 1.63A \tag{6-50}$$

The resonant parameters may be estimated once the equations governing the various modes are solved analytically. Fortunately as derived, each mode is governed by a set of linear differential equations that are readily solved using Laplace transform techniques. In particular, during Mode 2 when the resonant inductor current is charging up to approximately the minimum of the inductor current, the following holds:

$$i_r = \frac{V_{dc}}{L_r}t \tag{6-51}$$

Assuming that the inductor current does not change much during Mode 3, the resonant capacitor decays according to:

$$V_{cr1} = V_{dc}\cos\left[\sqrt{\frac{1}{L_r C_{r1}}}t\right] \tag{6-52}$$

while the resonant inductor current builds according to:

$$i_r = I_{Lmim} + V_{dc}\sqrt{\frac{C_{r1}}{L_r}}\sin\left[\sqrt{\frac{1}{L_r C_{r1}}}t\right] \tag{6-53}$$

Here, it is assumed that 't' starts at the end of Mode 2. For simplicity, the following equations will make similar assumptions that the symbol 't' is zero at the beginning of the respective mode. The time in Mode 4 is fixed by the delay between closing S_m and

opening S_a. The initial conditions for Mode 5 are $V_{cr2}(0) = 0$ and the resonant inductor current fixed at its maximum value $i_r(0) = i_{rmax}$. The value for i_{rmax} is found by evaluating (6-53) at the end of Mode 4. The equations governing Mode 5 are given by:

$$V_{cr2} = i_{r\max}\sqrt{\frac{L_r}{C_{r2}}}\sin\left[\sqrt{\frac{1}{L_r C_{r2}}}t\right] \tag{6-54}$$

$$i_r = i_{r\max}\cos\left[\sqrt{\frac{1}{L_r C_{r2}}}t\right] \tag{6-55}$$

If it is assumed that V_{cr2} charges up to V_{dc} prior to i_r decaying to zero, then the circuit enters Mode 5x. If it is further assumed that i_r decays to i_{r5} at the end of Mode 5, then the following holds for Mode 5x:

$$i_r = i_{r5} - \frac{V_{dc}}{L_r}t \tag{6-56}$$

Mode 6 is then entered and the main switch conducts until the control specifies that S_m open. If it is assumed that V_{cr2} has charged up to V_{dc} (as done above), then the circuit transitions to Mode 7b. Capacitor C_{r2} discharges and C_{r1} charges. At this point, the inductor current is at its maximum value and if it is assumed that the capacitor was sized sufficiently small so that the main inductor current does not appreciably change over this interval then:

$$V_{cr1} = \frac{I_{L\max}}{C_{r1} + C_{r2}}t \tag{6-57}$$

The above equations provide a blueprint for estimating the required resonant parameters. First of all, it is understood that the resonant portions of the cycle should be very small relative to the fundamental switching period. That is, the circuit should be in Mode 6 for approximately $D_o T_{sw} = 295$ μsec and in Mode 1 for approximately $(1\text{-}D_o)T_{sw} = 205$ μsec. To illustrate the sizing of the various parameters, it is reasonable to impose a limit of 4.8 μsec on the admissible time that the circuit operates in Mode 2. It follows from (5-36) that:

$$L_r = \frac{V_{dc}\,4.8\mu\,\text{sec}}{I_{L\min}} = .165mH \tag{6-58}$$

From (6-52) during Mode 3, it will take a quarter cycle for V_{cr1} to decay to zero. If this time is fixed at 14.3 μsec, then it follows that

$$\frac{\pi}{2}\sqrt{L_r C_{r1}} = 14.3\mu \text{ sec} \tag{6-59}$$

which results in

$$C_{r1} = .5\mu F . \tag{6-60}$$

During this quarter cycle, the resonant inductor current builds to a maximum established from (6-53)

$$i_{r\max} = I_{L\min} + V_{dc}\sqrt{\frac{C_{r1}}{L_r}} = 4.28A . \tag{6-61}$$

The remaining parameter is C_{r2}. It is understood that during Mode 7b, the voltage V_{cr1} must rise to V_{dc}. Imposing a time constraint of 46.7 μsec and plugging into (6-57):

$$V_{cr1} = \frac{i_{L\max}}{C_{r1} + C_{r2}} 46.7\mu \text{ sec} = 50.8V \tag{6-62}$$

and solving for C_{r2} yields:

$$C_{r2} = 1\mu F \tag{6-63}$$

Not having used the modeling equations for Modes 5 and 5x, it is appropriate to return to them and examine how much time the circuit operates in those two modes.

$$V_{cr2} = i_{r\max}\sqrt{\frac{L_r}{C_{r2}}}\sin\left[\sqrt{\frac{1}{L_r C_{r2}}}t\right] = 50.8V \tag{6-64}$$

Solving for the time required for V_{cr2} to charge to 50.8V yields:

$$t_5 = 15.14\mu \text{ sec} \tag{6-65}$$

During t_5 equation (6-55) predicts that i_r decays down to:

$$i_{r5} = 1.64A \tag{6-66}$$

Therefore, since i_r has not decayed down to zero, the circuit enters Mode 5x and the required decay time is found from (6-56) to be:

$$t_{5x} = \frac{i_{r5}L_r}{V_{dc}} = 5.31\mu \text{ sec} \tag{6-67}$$

If resonant parameter values L_r = .165 mH, C_{r1}= 0.5 μF, and C_{r2} = 1.0 μF are not acceptable (as shown by simulation), then the process can be iterated.

F. PSPICE SIMULATION

Figure VI-13 illustrates the Joung topology modeled in PSPICE with the circuit components derived above.

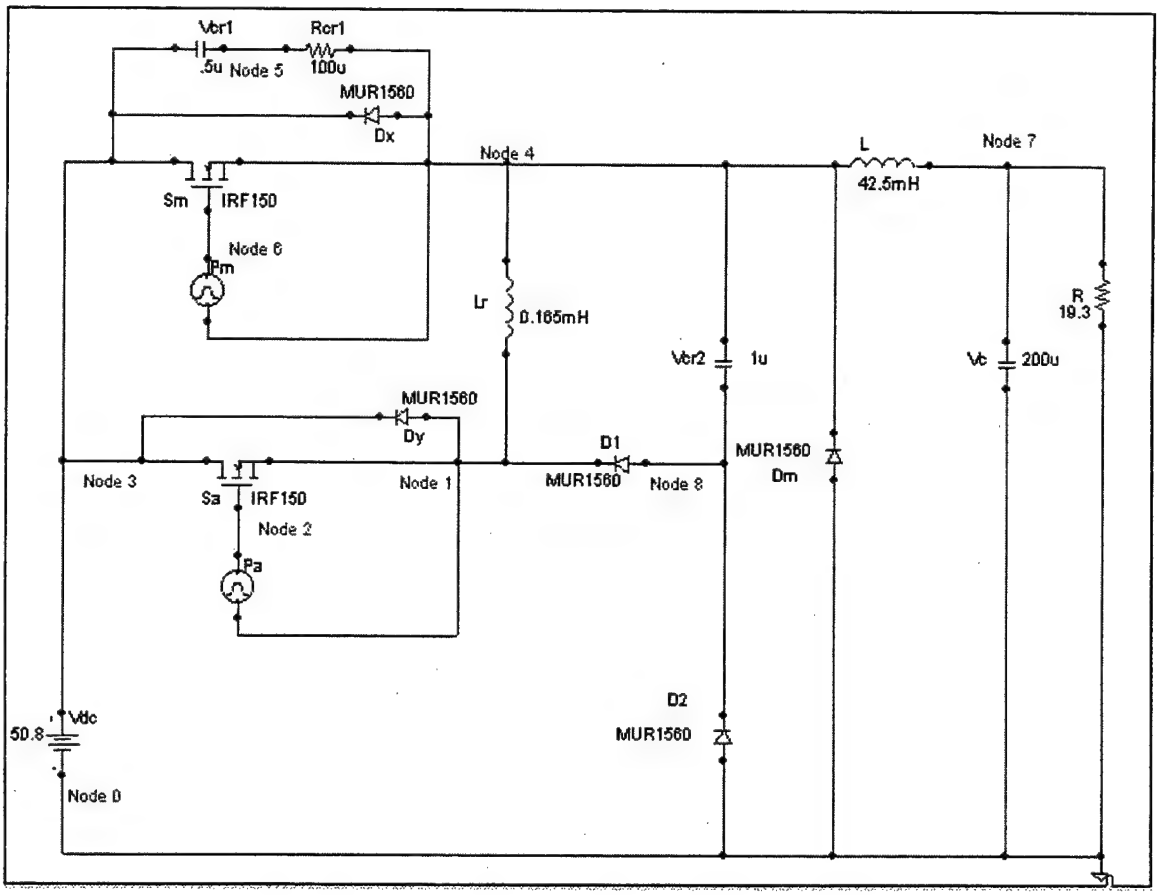

Figure VI-13 Joung Topology PSPICE Model

1. Circuit Component Selection

The predetermined circuit component values are C_{r1} = 0.5 μF, C_{r2} = 1.0 μF, R = 19.3 ohms, L_r = .165 mH, and L = 42.5 mH. R_{cr1} is assigned a small resistive value to prevent the main switch S_m from being placed directly across C_{r1}. Earlier the following elements were described and are described briefly here again for convenience. MUR1560 diodes were selected for their low stored charge and ultra-fast recovery characteristics. The IRF150 is a n-channel enhancement-mode silicon power field-effect transistor designed for switching applications.

2. Simulation Evaluation

a) Switch Gating

The switching frequency (f_s) remains fixed at 2kHz. A duty cycle (D) of 50% is set for the main switch, D_{Sm}, and a duty cycle of 20% is set for the auxiliary switch, D_{Sa}. The gating signals used in this model are shown in Figure VI-14. Ten-volt square wave pulses are used to gate the IRF150 transistors and their amplitudes are shown here by taking the difference in the node voltages across each pulse generator.

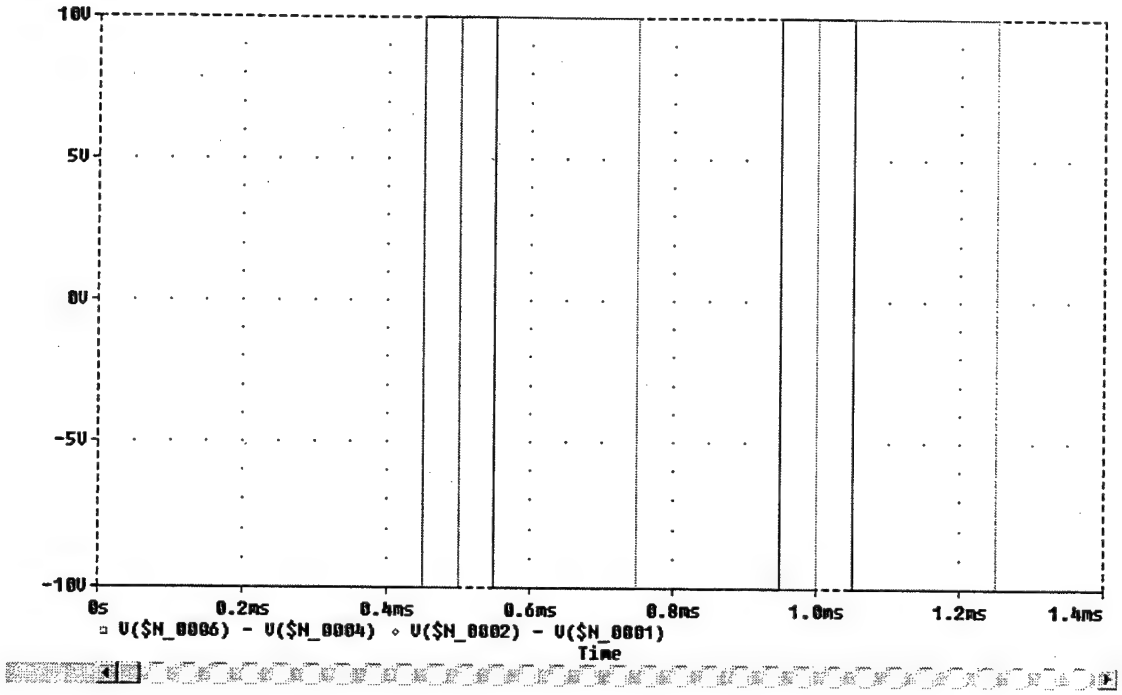

Figure VI-14 Switching Frequency

The auxiliary switch, S_a, is the first switch gated which places the circuit into Mode 2. An initial S_a gate pulse is delayed (t_{DSa}) for 0.45 msec. The auxiliary switch pulse width (PW_{Sa}) is shown below in (6-68). The period (T) is found from (6-67).

$$T = \frac{1}{f_s} = 0.5m\sec \tag{6-67}$$

$$PW_{Sa} = D_{Sa}T = 0.1m\sec \tag{6-68}$$

The auxiliary switch, S_a, closes every 0.5msec (from (6-67)); therefore, S_a closes at 0.45, 0.95, 1.45, 1.95, 2.45, 2.95ms… and opens at 0.55, 1.05, 1.55, 2.05, 2.55, 3.05ms…

The main switch, S_m, is closed at the end of Mode 3, which is the beginning of Mode 4. The initial S_m gate pulse is delayed (t_{DSm}) by 0.5msec. The main switch pulse width (PW_{Sm}) is as calculated in (6-69).

$$PW_{Sm} = D_{Sm}T = 0.25m\sec \tag{6-69}$$

The main switch, S_m, closes every 0.5msec; therefore, S_m closes at 0.5, 1.0, 1.5, 2.0, 2.5, 3.0ms… and opens at 0.75, 1.25, 1.75, 2.25, 2.75, 3.25ms…

The voltage across the load is depicted in Figure VI-15. The voltage levels out at approximately 31V at 40ms.

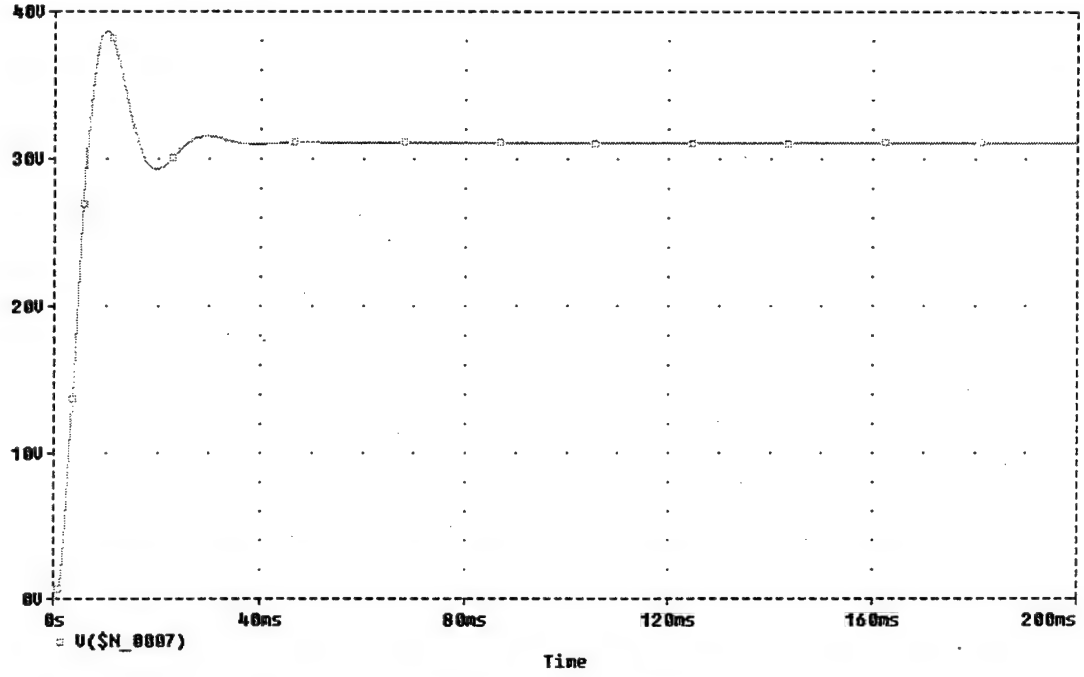

Figure VI-15 – Load Voltage

b) Switch Performance

The auxiliary switch closes at 49.45ms as shown by the 'square' marked line in Figure VI-16. The voltage across S_a is at a maximum value when it closes, but the current through (S_a) shows soft-current switching in the same figure. S_a turns on softly due to the gradual increase in current through the switch.

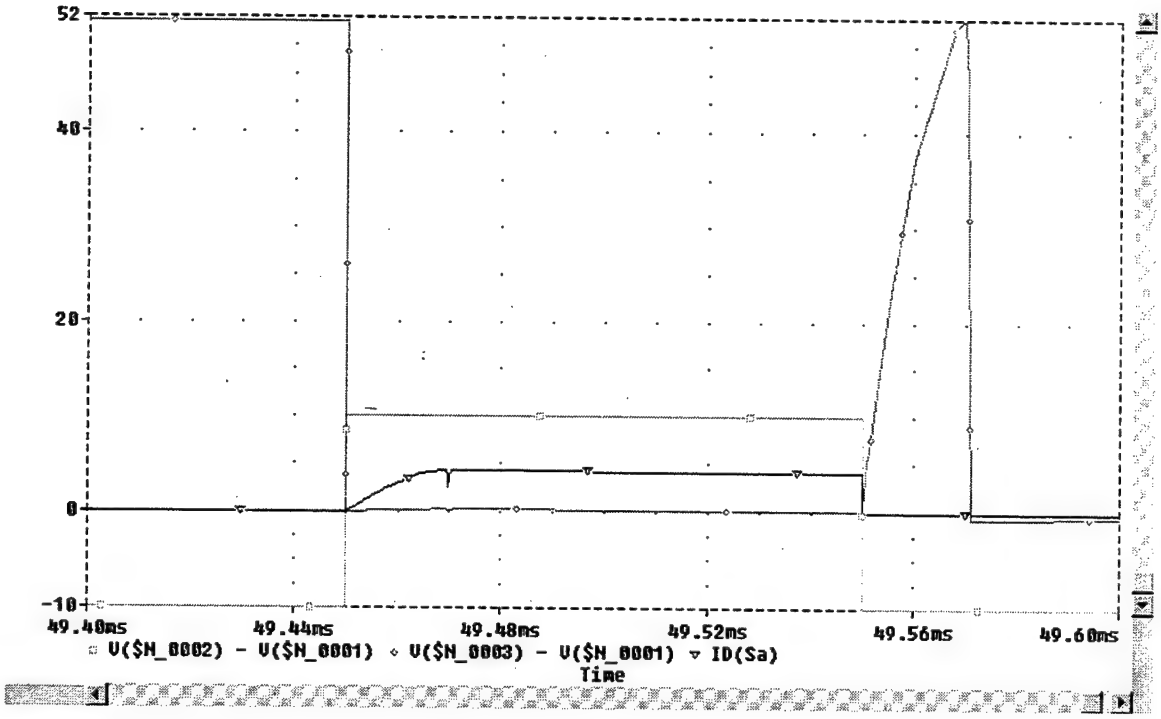

Figure VI-16– Auxiliary Switch Characteristics

The main switch closes at 49.5ms as shown by the 'square' marked line in Figure VI-17. Zero-voltage-switching (ZVS) is realized across S_m as seen in the same figure. The voltage across the main switch reaches zero approximately 0.025ms prior to S_m closing.

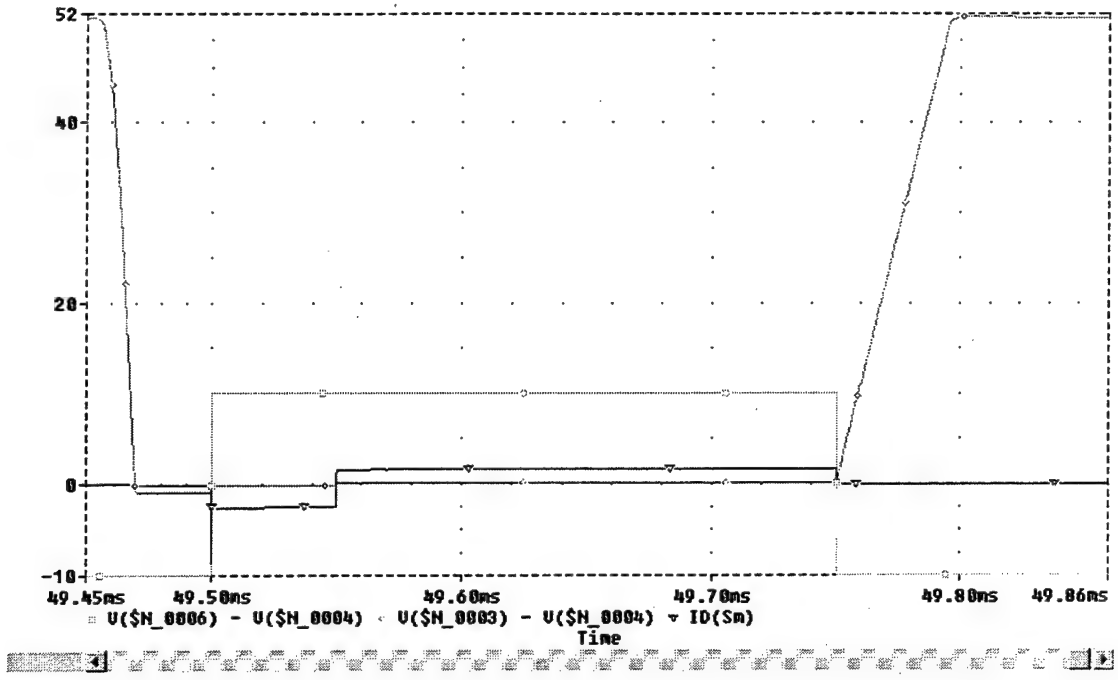

Figure VI-17 – Main Switch Characteristics

c) Circuit Efficiency

The efficiency of the circuit is easily obtained by dividing the output power by the input power. An efficiency of 95.1% is obtained at time equal to 200ms as illustrated in Figure VI-18.

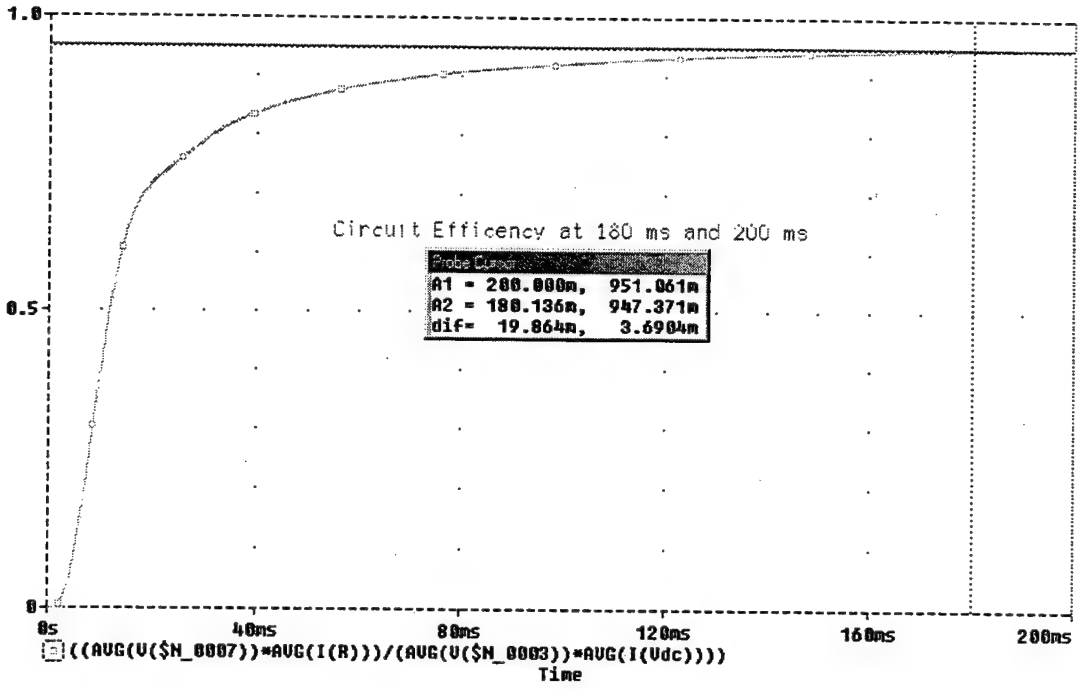

Figure VI-18 – Circuit Efficiency

The output ripple voltage for the circuit is found by looking at the final period of the 200ms PSPICE run. From Figure VI-19, the ripple is determined by subtracting the peaks of the waveform and dividing the result by the output voltage as given in (6-70).

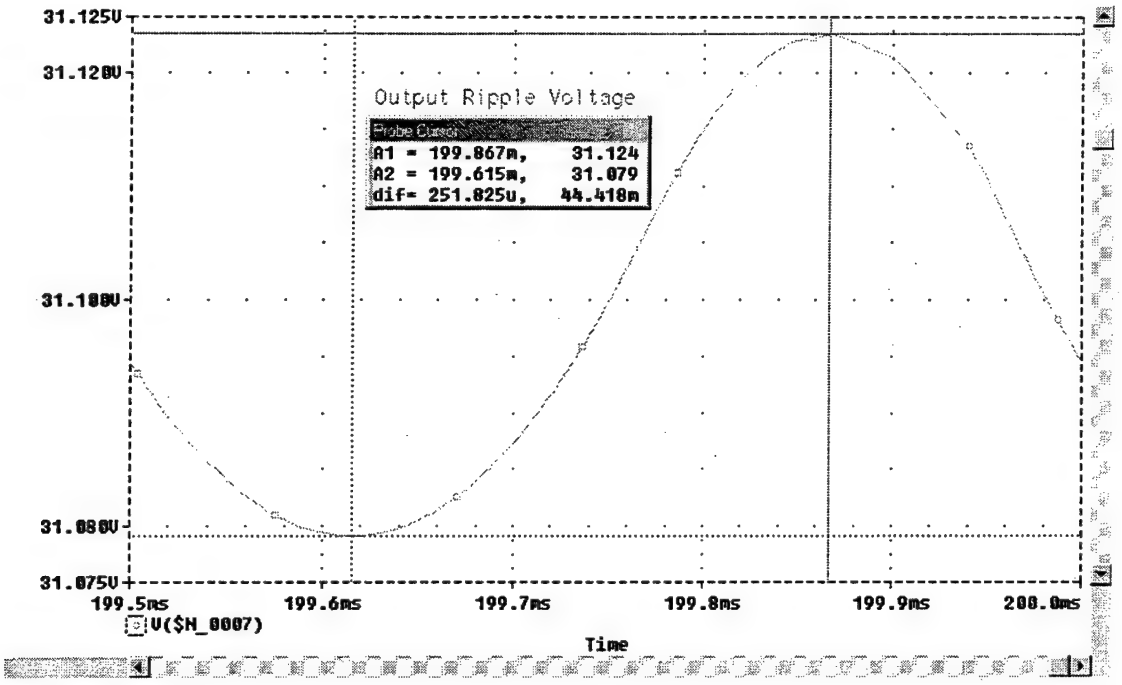

Figure VI-19 – Output Ripple Voltage

$$\%Ripple = 100 \times \frac{PositivePeak - NegativePeak}{OutputVoltage} = 100 \times \frac{31.124 - 31.079}{31.095} = 0.52\% \quad (6\text{-}70)$$

G. LABORATORY TOPOLOGY TESTING

1. Introduction

The following section presents some of the details from the construction and testing of a low-frequency soft-switched converter similar to that outlined in the paper by G. B. Joung [12]. Specifically noted are:

- Step-by-step descriptions of how the 2 kHz buck resonant converter was set up in the lab.
- Basic descriptions of how the circuit should operate.

- An outline of the testing process performed in the lab from which optimum values for the circuit components were derived.
- Summary and future work.

2. Circuit Setup

a) Gather Equipment

- (1) InverPower Logic Power Supply
- (1) InverPower 6 Channel Pulse Amplifier
- (1) Variac
- (1) InverPower Power Diode Rectifier
- (1) InverPower Filter Capacitor
- (1) InverPower 3-Phase Voltage Source Inverter
- (1) Tektronix DM2510 Digital Multimeter
- Circuit components:

  L: InverPower 42.5 mH

  L_r: 0.165 mH inductor

  C: (2) 100 μF, 240 VAC electrolytic capacitors

  C_{R2}: Various electrolytic capacitors ranging from 1 to 10 μF

  Diodes D_1, D_2, D_m: (3) Motorola MU1560

  R: InverPower 3kW – 115 ohm Resistor Load
- Any measuring equipment deemed necessary

b) Setup Triggering Circuit

One function generator is designated as the main and one as the auxiliary for triggering the main and auxiliary switches respectively. Connections and settings

were made as follows:

- Connect the trigger and burst port on the rear of the main unit to the transistor-transistor-logic port on the rear of the auxiliary unit.
- Set both mode dials to normal.
- Set both frequency range dials to 2K.
- Set both waveform dials for square positive pulse.
- Set both DC offset knobs to 12 o'clock.
- Adjust both amplitude knobs to full CW.
- Set main duty cycle to about 50% and auxiliary duty to between full CCW and 20%.
- Set the main start phase knob to "$-\pi/2$" and auxiliary start phase knob to 12 o'clock.

Setting up the function generators as described above allows the falling edge from the auxiliary unit to trigger the rising edge of the main unit ninety degrees before the auxiliary pulse turns off. In this respect, the function generator designated as auxiliary acts as master, and the designated main acts as slave. The overall duty cycle will be about 55%.

One must next connect the main and auxiliary function generator outputs to the input jack of a 'Pulse Amplifier'. Subsequently, one must connect the +24V and -15V from the 'Pulse Amplifier' to the 'Logic Power Supply'.

The operator must then connect the main channel output from the 'Pulse Amplifier' to the base of T1 on the 'Voltage Source Inverter'. The auxiliary channel output must then be connected from the pulse amplifier to the base of T5 on the 'Voltage Source Inverter'.

Note: It was discovered that the snubber capacitor associated with switch T1 was blown in the voltage source inverter. Presence of a snubber capacitor, which is normally part of the switch inside the 'Voltage Source Inverter', would seriously impede circuit operation.

c) Setup Power Supply Circuit

One phase from the variac output must be connected to one phase of the 'Power Diode Rectifier' input. The positive and negative terminals from the 'Power Diode Rectifier' are then connected to the positive and negative terminals of the 'Filter Capacitor'.

One must then connect all six resistors of the resistor load in parallel using shorting bars. This gives a load resistance value of 19.3 ohms. The negative terminal of the 'Filter Capacitor' is connected to the bottom row of the shorting bars on the resistor load. The operator must connect the positive terminal from the 'Filter Capacitor' to the positive terminals of T1 and T5 on the 'Voltage Source Inverter'. After that, the power supply and switching portion of the circuit is set up as shown in Figure VI-20.

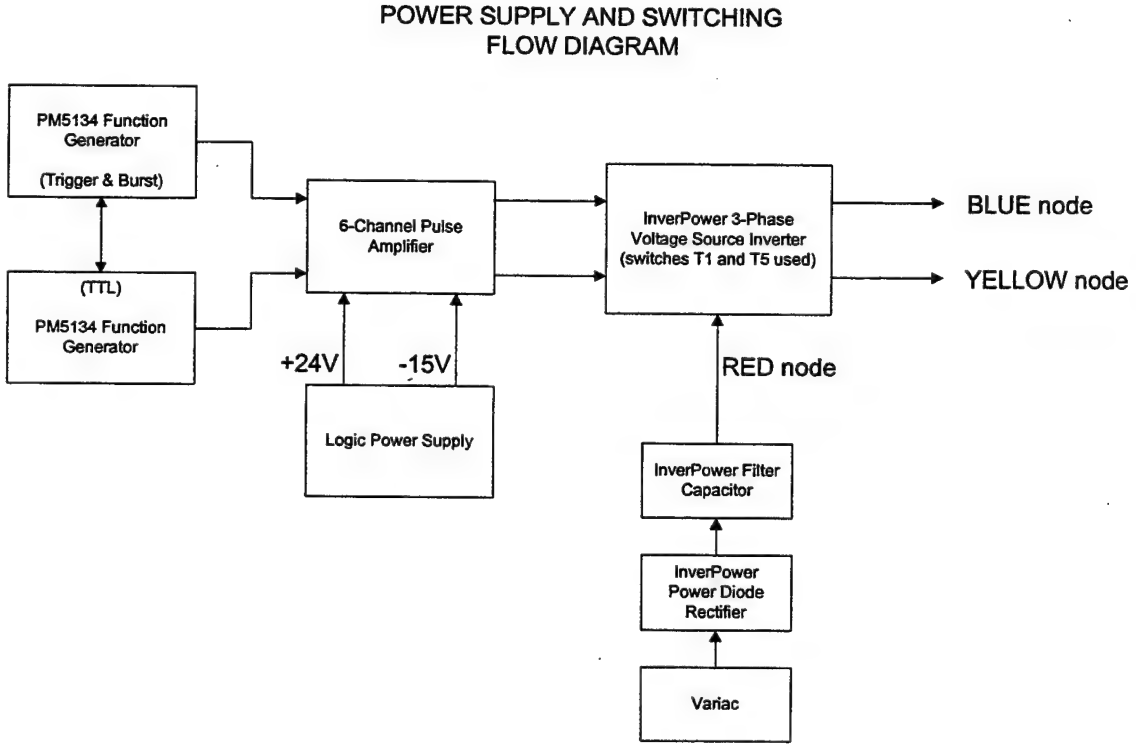

Figure VI-20 Power & Switching Flow

d) Setup Soft-Switched Buck Circuit

Each diode is prepared by soldering cable connectors to the anode and cathode of all three MUR 1560 diodes. The circuit fabricator then bolts the cable connectors to the common and 100% points of the 42.5 mH inductor to be used as the main inductor, L.

Next, the color codes for the banana wires that connect the circuit components were chosen. Colors were chosen arbitrarily for the circuit, except that black was used for ground and red was used for voltage source output. Connect the nodes as follows.

- Blue node connects: 1) Main switch emitter, 2) C_{R2}, 3) Main diode, D_m cathode, 4) Resonant Inductor L_R, and 5) Main Inductor L
- Green node connects: 1) C_{R2}, 2) Diode, D_1 anode, and 3) Diode, D_2 cathode
- Yellow node connects: 1) Auxiliary switch, S_a emitter, 2) Main Inductor, L_R, 3) Cathode of diode D_1
- Indigo node connects: 1) Main Inductor L, 2) Load resistor R, 3) Load Capacitor C
- Red node connects: 1) Main switch, S_m collector, 2) Auxiliary switch, S_a collector, 3) Voltage source output
- Black node connects: 1) Anode of main diode D_m, 2) Anode of diode D_2, 3) Load resistor R, 4) Load Capacitor C, 5) Voltage source ground

A color-coded circuit schematic is shown in Figure VI-21.

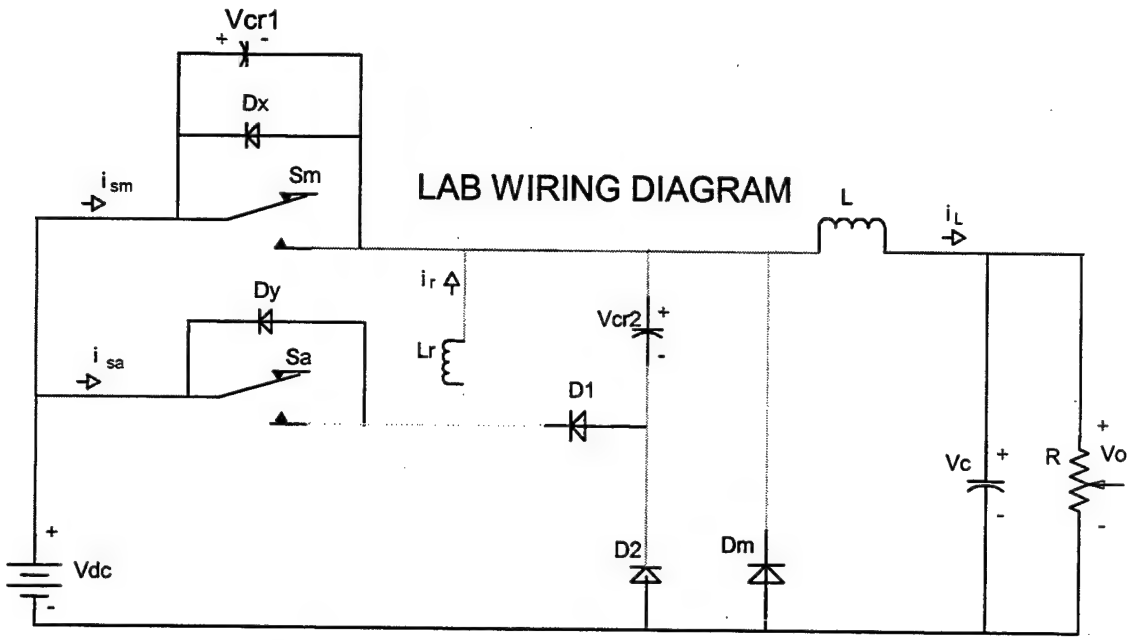

Figure VI-21 – Lab Wiring Diagram

3. Test Procedures Performed

The ultimate goal of this project is to build a high-voltage, high-frequency version of this resonant converter. A low-voltage, low-frequency model was constructed in the lab in order to make observations on system behavior. The following discussion outlines the process used in developing the low voltage / low-frequency system.

a) Initial Setup

The switching frequency for the low-frequency model was determined to be 2 kHz. Resistive load R was chosen at 19.3 Ω. A small R was chosen in order to observe circuit operation at maximum load. Main inductor, L, was 21.25 mH, which is more than four times L_{CRIT}. Resonant inductor, L_R, was 2.125 mH initially, 1/10 the value of L. Load capacitance, C, was set at 200 μF; resonant capacitance C_{R2} was 10 μF. A snubber capacitance of 1μF was placed in line with the switches internal to the 'Voltage

Source Inverter' and assumed sufficient for C_{R1}. Values presented in Joung's paper were scaled for 2 kHz switching to determine the component values for the lab.

b) Inductance Values Modified

The circuit was built using the above values. The first observation was that after auxiliary switch turn-on, too much time was required for i_{LR} to ramp up to i_L. To correct this, L_R was reduced to .165 mH. L was also increased to 42.5 mH because it was thought that larger main inductance would only be beneficial to circuit operation.

c) Capacitance Values Modified

Figure VI-22 displays trace one with $C_{R2} = 10\ \mu F$.

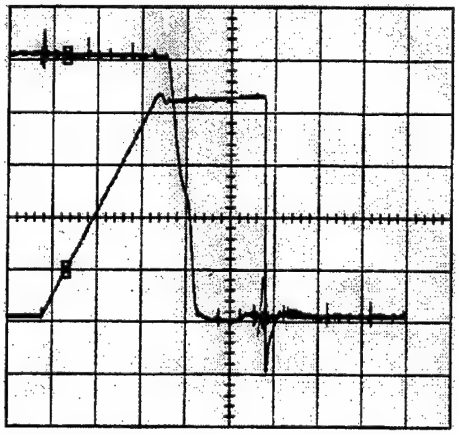

Figure VI-22

Upper trace: V_{Sm} vs. time (10 V/div)

Lower trace: I_{Sa} vs. time (0.5 A/div)

Time scale: 20 μs/division

This plot shows auxiliary switch turn-on at 18 μs and main switch turn-on at 70 μs. Note the i_{Sa} ramp-up, which follows auxiliary switch turn-on. The slope of this ramp was made steeper by using a smaller L_R. Also note that the S_a is closed 52 μs before S_m closes. Since the S_a duty cycle is 20%, the total S_a on time is 100 μs. The S_m pulse is triggered 52 μs after S_a (1/2 of the S_a on time) as desired.

$V_{OUT} = 29.9$ V $\quad I_{OUT} = 1.61$ A

$V_{IN} = 50.8$ V $\quad I_{IN} = 0.99$ A

$\eta = 94.76\%$

Figure VI-23 displays trace two with C_{R2} = 10 μF.

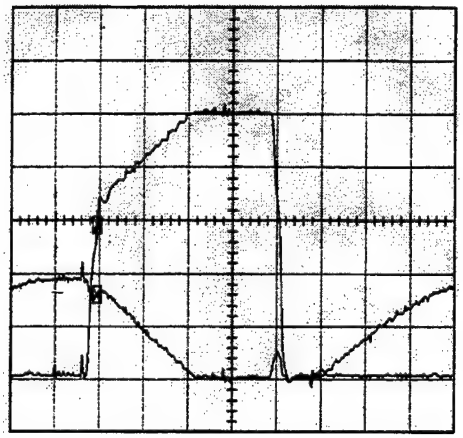

Figure VI-23

Upper trace: V_{Sm} vs. time (10 V/div)

Lower trace: V_{CR2} vs. time (10 V/div)

Time scale: 50 μs/division

This plot shows main switch turn-off at 80 μs and main switch turn-on at 295 μs. This tells us operating of S_m is at approximately a 43% duty cycle. The voltage across C_{R2} reaches only 20 V.

Figure VI-24 displays trace three with $C_{R2} = 2\ \mu F$.

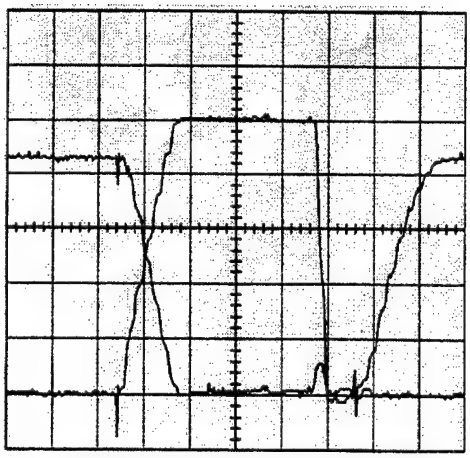

Figure VI-24

Upper trace: V_{Sm} vs. time (10 V/div)

Lower trace: V_{CR2} vs. time (10 V/div)

Time scale: 50 μs/division

This plot shows main switch turn-off at 125 μs and main switch turn-on at 340 μs. Notice here that V_{CR2} reaches 40.3 V with a smaller C_{R2} but still falls short of reaching full source voltage when the main switch is off. The time required for main switch voltage to reach the source voltage after turn-off is about 20 μs compared to 40 μs when using $C_{R2} = 10\ \mu F$.

$V_{OUT} = 29.4$ V $\quad$ $I_{OUT} = 1.59$ A

$V_{IN} = 50.8$ V $\quad$ $I_{IN} = 0.97$ A

$\eta = 94.87\%$

Figure VI-25 displays trace four with C_{R2} = 1 μF.

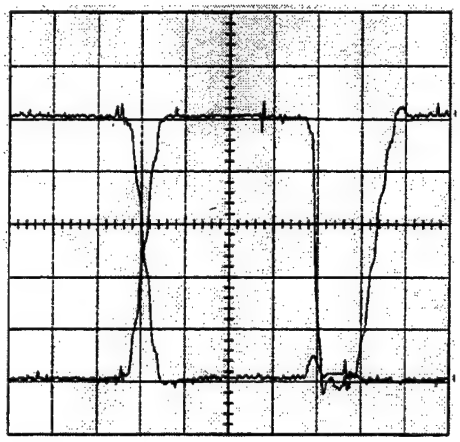

Figure VI-25

Upper trace: V_{Sm} vs. time (10 V/div)

Lower trace: V_{CR2} vs. time (10 V/div)

Time scale: 50 μs/division

This plot shows main switch turn-off at 125 μs and main switch turn-on at 340 μs. Here C_{r2} charges to V_{dc} before main switch turn-off as desired. Note C_{r2} does not exceed V_{dc} as it is limited as described in Mode 5x. If C_{r2} does not charge to V_{dc}, current flows through V_{cr1} as described in Mode 7a. This current flow through V_{cr1} decreases the efficiency. While it is desired that C_{r2} charge to V_{dc}, it is not desired to charge to quickly as this causes current to circulate through D_1 and D_2 as described in Mode 5x. Because of this, there is a delicate balance in the selection of C_{r2} to obtain the maximum possible circuit efficiency.

V_{OUT} = 29.9 V I_{OUT} = 1.61 A

V_{IN} = 50.8 V I_{IN} = 1.0 A

η = 94.76%

4. Comments on Efficiency

Overall converter efficiency for each value of capacitance (10 μF, 2 μf, and 1 μF) was computed. All efficiency measurements fell between 94% and 95%. These efficiency values can be explained in part by measurement tolerances and are too close to draw conclusions about changing efficiency resulting from changing the capacitance values as described.

These efficiency numbers take into account switching losses as well as conduction losses. It will be interesting to observe efficiency in the high-frequency version of this circuit. If this converter truly operates soft-switched, there will be a minimal increase in switching losses at higher switching frequency.

It should be noted that a small resistive load was used in this circuit, thus efficiencies calculated here are close to the minimum.

5. Summary and Future Work

Circuit components for the high-frequency version of this converter should be chosen with the following constraints in mind:

- Normally it would be assumed that large main inductance and output capacitance should be large, but the whole idea behind increasing switching frequency is to reduce the size of these two components.
- L_R should be small to minimize main switch voltage rise time, but reasonably large enough to charge C_{r2}.
- Optimal circuit operation should occur with only parasitic capacitance in the switch. This means making the 'external' C_{r1} equal to zero.
- Too large of C_{r2} relative to L_r will decrease circuit efficiency by causing current to flow through C_{r1}. Too small of C_{r2} will lower efficiency by causing excessive D_1 and D_2 conduction.

As stated above, future work will involve the construction of the same circuit with a higher switching frequency. Part of any future work may also include derivation of some specifications for C_{r2} values with respect to other circuit parameters.

Further work should also involve evaluation of the circuit under different load conditions. One of the original goals of this project was to develop a switching converter that had minimum switching losses when operating at full load.

VII. CONTROLLER DEVELOPMENT

A. APPROACH TO LOGIC CONTROL

Proportional plus Integral (PI) control was selected for its simplicity and excellent steady-state error properties. A negative feedback control loop was developed based on commanding the output load voltage. Initially control was developed for a single-switched buck converter. This would require only analog control. Once the single-switch was mastered, a second switch could be added and the task of dual switch control could be tackled.

B. CONTROLLER ALGORITHM DERIVATION

First, the PI control block diagram was developed as illustrated in Figure VII-1.

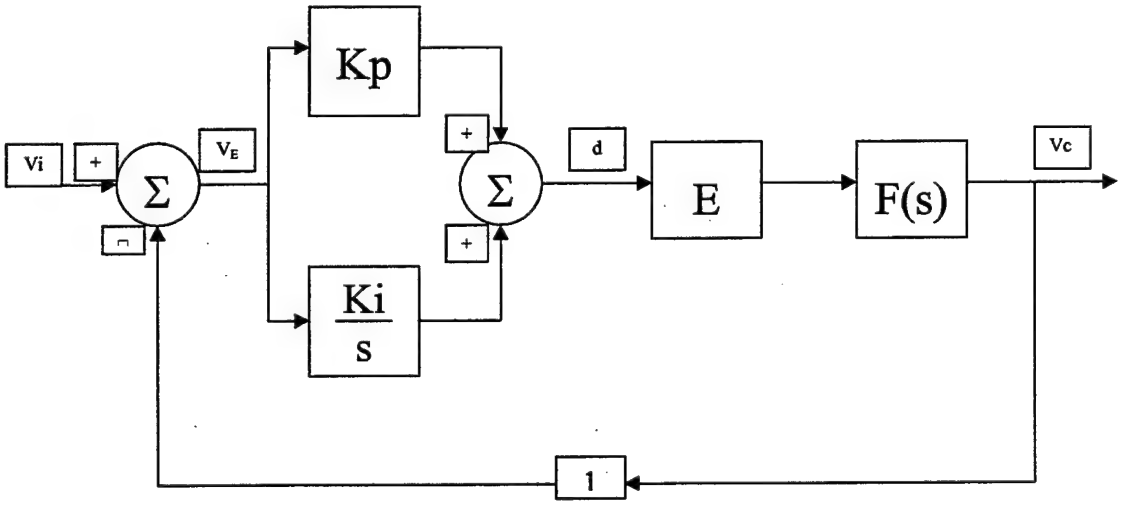

Figure VII-1 Proportional Integral Control Block Diagram

C. POLE SELECTION

An equation for pole placement was developed utilizing the block diagram in Figure VII-1 and poles were chosen. Once an equation was developed, a MATLAB program was written. The equation and MATLAB program are contained in Appendix A. The three poles were selected based approximately on Butterworth criteria: -1325, -675 +/- j1200 rad./sec. From the MATLAB program, the results defined the capacitor C and the gains Ki, and Kp as shown in Appendix B. The pole placement is shown in Figure VII-2

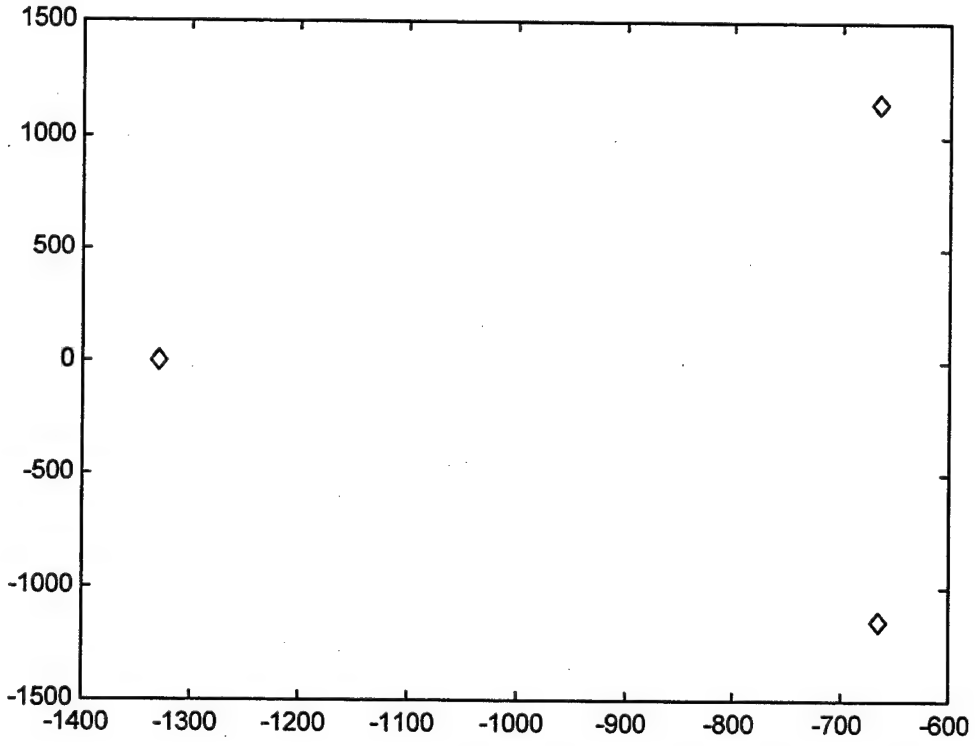

Figure VII-2 Pole Placement

D. CONTROLLER IMPLEMENTATION

1. The Single-Switch Approach

To implement the control block diagram, 741 operational amplifiers were chosen. With gains and capacitance C established by pole placement, the single-switch converter loop was closed with the use of an LM111 comparator and an optical isolator for the switch gating. The LM111 was use to compare a 12V triangle wave with the commanded duty cycle.

The single-switch controller was developed and tested at switching speeds of 2kHz and 5kHz. Shown below in Figure VII-3 is the single-switch controller at a 2kHz switching speed. Because the two-switch converter will operate with the same dependence on duty cycle as the single-switch converter, once the single-switch control gains are established, only the second switch and PWM need to be added.

The second switch will need to be pulsed at the same rate as the main switch but with a different duty cycle.

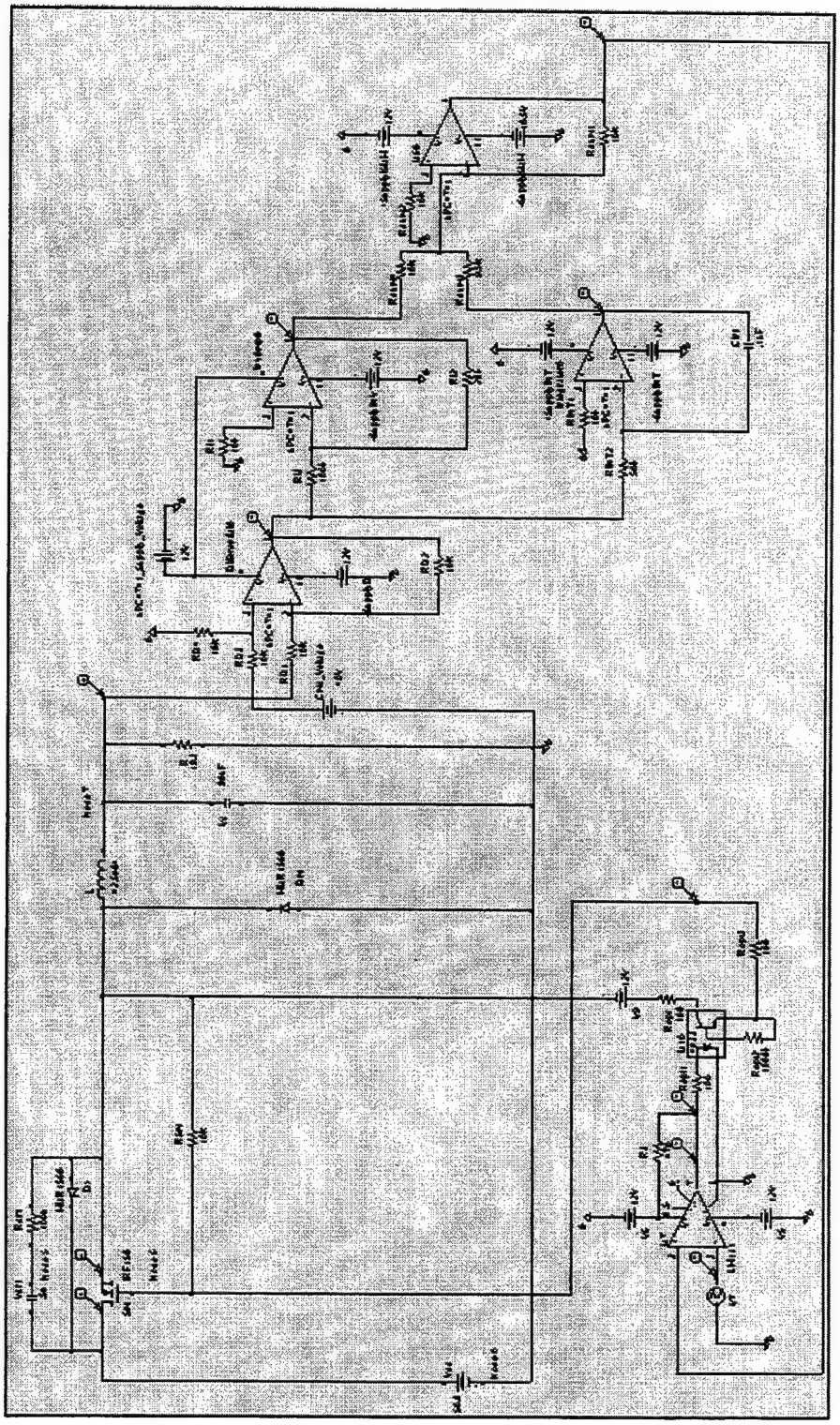

Figure VII-3 Single-Switch Controller

In order to demonstrate the operation of the control, a 40V command signal was used in PSPICE. From Figure VII-4, the output voltage is indeed 40V indicated by the (+) output voltage line. The output voltage ripple is < .01% in the viewed 1ms time frame. Other output voltages are included in the figure to demonstrate the stability of the control system.

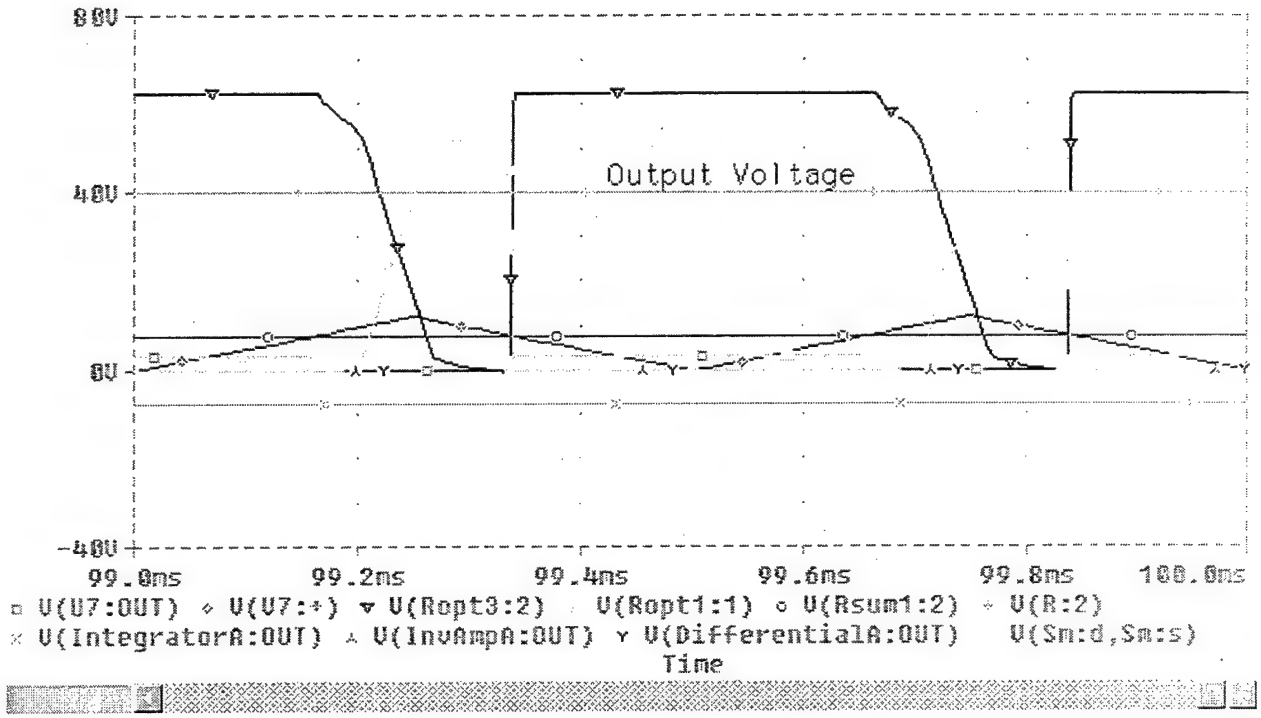

Figure VII-4 Single-Switch Controlled Output Voltage

2. The Addition of the Second Switch

Having an operational single-switch controller allowed for the addition of a second switch with the confidence of knowing that the 741 amplifier gains were properly set. No further gain determinations or modifications were required.

A key factor that must be addressed with the two-switch implementation is the order and timing of the switches. The auxiliary switch (Sa) must be fired first and the main switch (Sm) must be fired prior to the auxiliary switch turning off. A control system must be developed that will maintain the desired firing arrangement. To accomplish this an exclusive-or is required. In Figure VII-5, a means for ensuring a proper firing order of the switches is shown. The auxiliary switch is fired first from the output of a single timer. Here it is shown as a 0.1ms pulse out of the auxiliary switch timer (Timer Sa). The duty cycle pulse established from the output of the LM111 comparator is passed through the exclusive-or circuit with the main switch timer output. The main switch timer output is shown here as a 0.05ms pulse. The exclusive-or output is used to pulse the main switch. From this setup the auxiliary switch will always fire first and the main switch will fire second with varying pulse widths depending on the commanded duty cycle. This firing order will ensure the circuit is soft-switching.

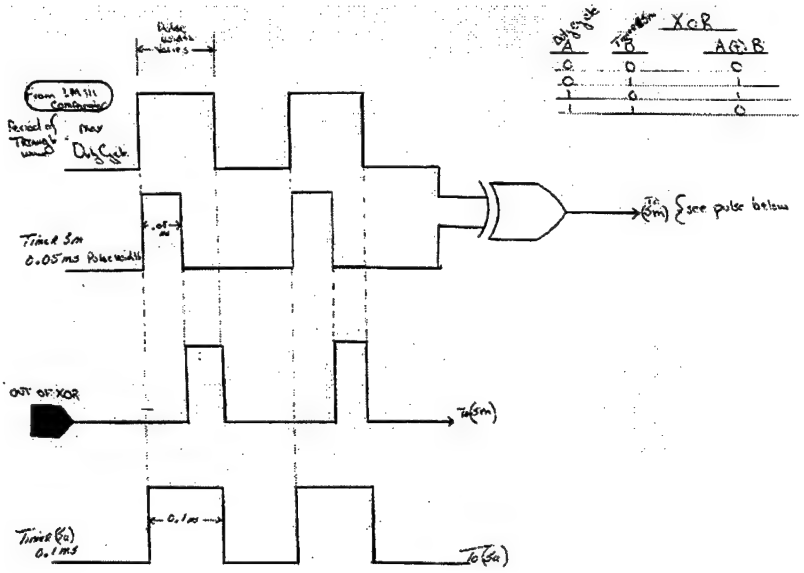

Figure VII-5 Logical XOR Requirement

Now that the method of firing is established, a means for accomplishing this task is required. Initially it was intended that mixed logic would be used within the control. CMOS exclusive-or technology was proposed. After much thought and many trials with ORCAD's release of version 9.1 A/D, it was determined that the learning curve required to complete the simulation was too great and hindered progress. Efforts were then focused on developing a purely analog controller so that a familiar existing version of MicroSim's PSPICE owned by the Naval Postgraduate School could be used for the remainder of the developmental process.

Remembering that the implementation means desired is analog, a set of optical isolators is chosen to implement the exclusive-or circuit. The two-switch control circuit is shown in Figure VII-6. The A4N25 optical isolators (U17 and U32) are tied in a manner such that their input diodes are opposing each other. The output of buffer-A and the main switch timer (TSm) are connected so that the output creates an exclusive-or circuit. This formation allows for a total analog control system.

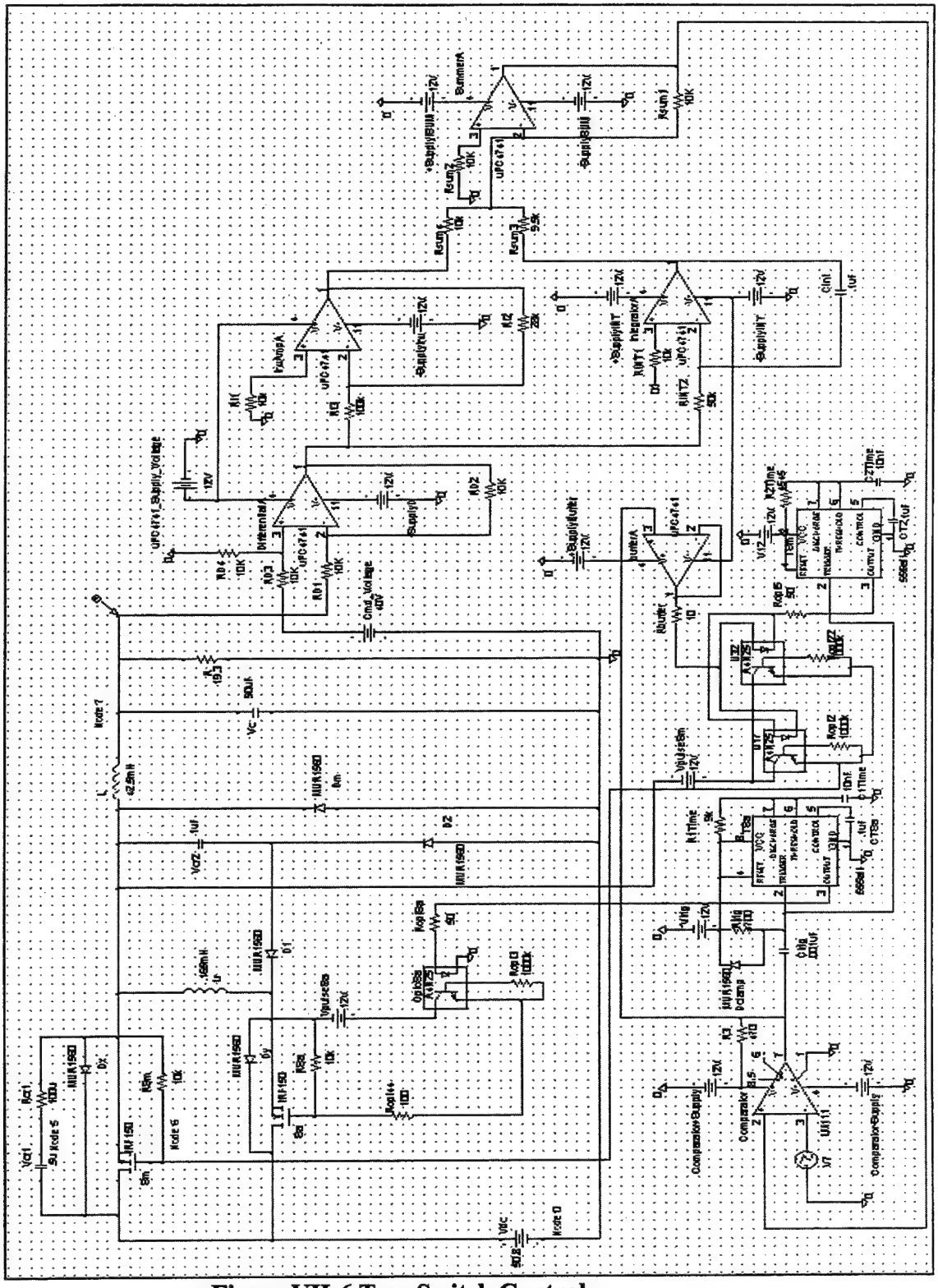

Figure VII-6 Two-Switch Control

E. CONTROLLER SIMULATIONS AND TUNING

1. Command Voltage Testing

The switching order is established as stated above. The circuit is configured as shown in Figure VII-6 and needs to be simulated in order to demonstrate the idea. Initially PSPICE gave convergence errors, as is often the case. It was discovered that the optical isolators were very sensitive to the amounts of current required in order to produce a properly biased internal BJT. Because of this a separate circuit was developed with only an optical isolator and IRF150 switch. After fine-tuning the bias points, the values required were transferred over to the complete control model. The first test of the controller consisted of holding the load constant and applying a command voltage of 30V. The output results are shown in Figure VII-7.

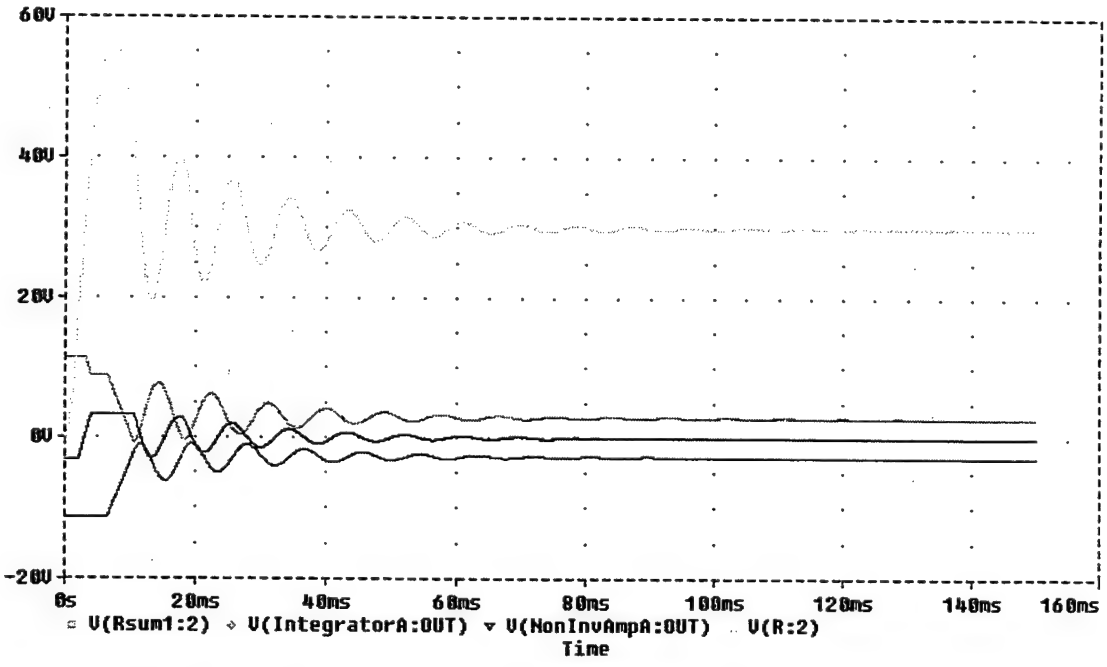

Figure VII-7 Commanded 30V Output Voltage

The output voltage is given in the figure by Δ and is indeed settling out to the commanded 30V. The percent ripple is ≅ 0.3% and shown in Figure VII-8.

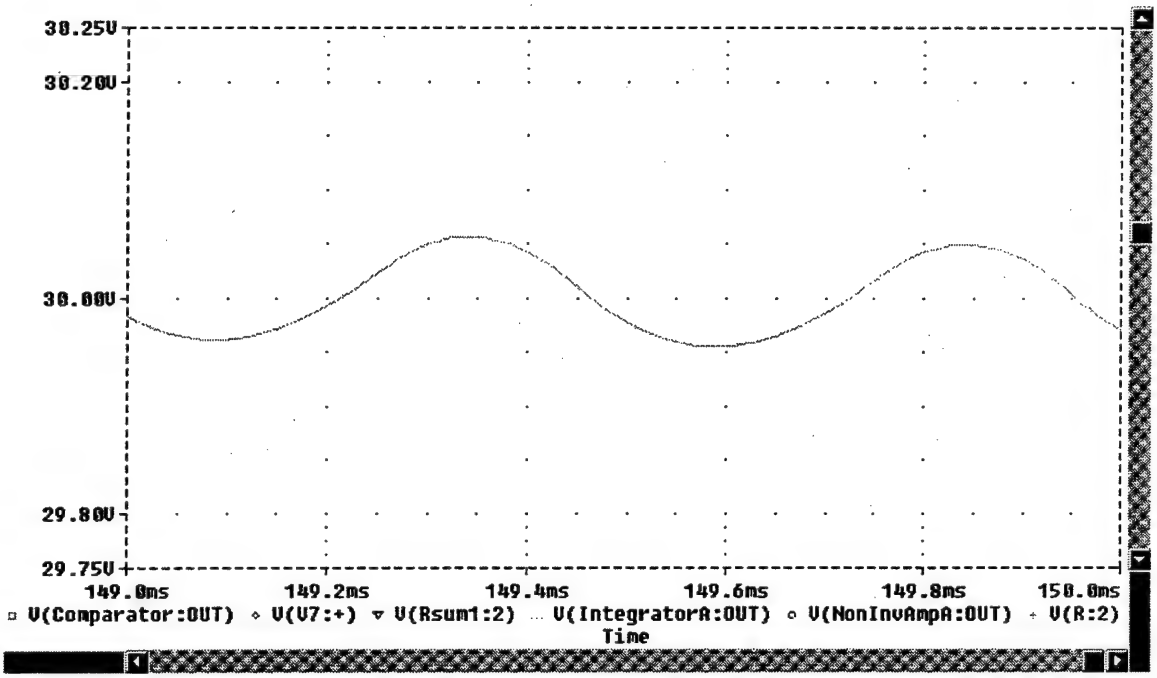

Figure VII-8 Commanded 30V Output Ripple

The percent ripple is determined by the value of capacitor 'C' as discussed in the buck converter operation section. Because the value of 'C' also determines pole placement, the selection of 'C' must be chosen carefully. Under conditions of lower command voltages the value of 'C' may need to be increased to provide for the desired minimum output voltage ripple.

Next a command voltage of 40V was tested. All other component values were held constant. The circuit was simulated and the output voltage was observed. The observed output voltage can be seen in Figure VII-9. Approximately 80ms elapse before the circuit voltage settles to 40V with the requisite ripple level.

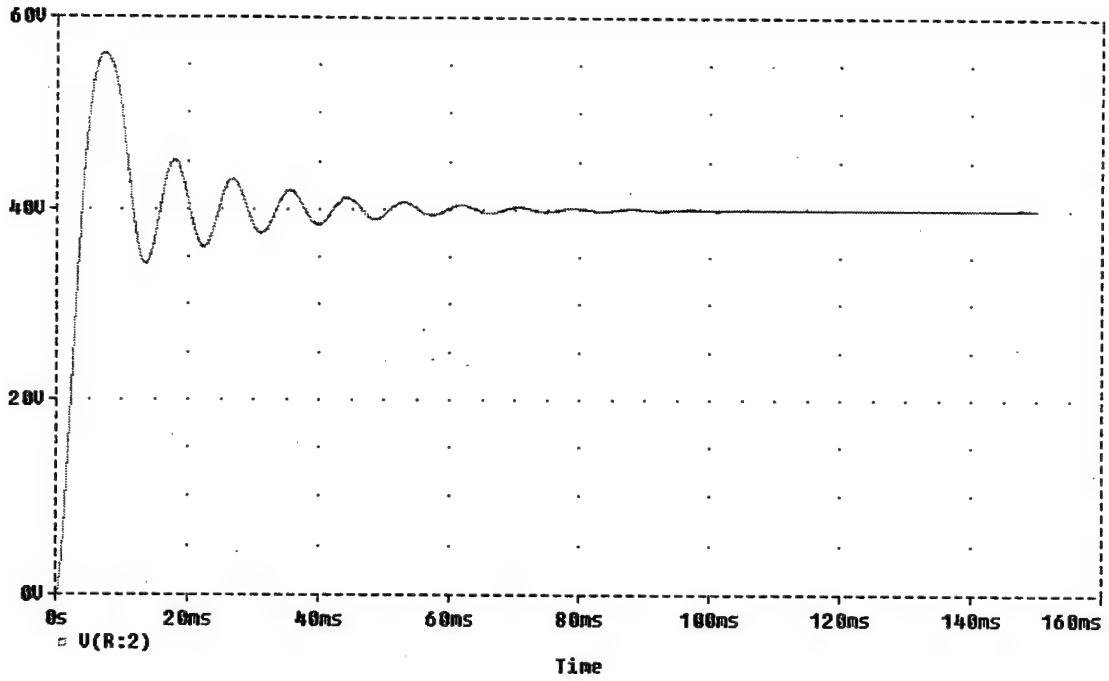

Figure VII-9 Commanded 40V Output Voltage

In Figure VII-10 the output voltage ripple is displayed. The ripple displayed here is $\cong 0.2\%$ at 149ms.

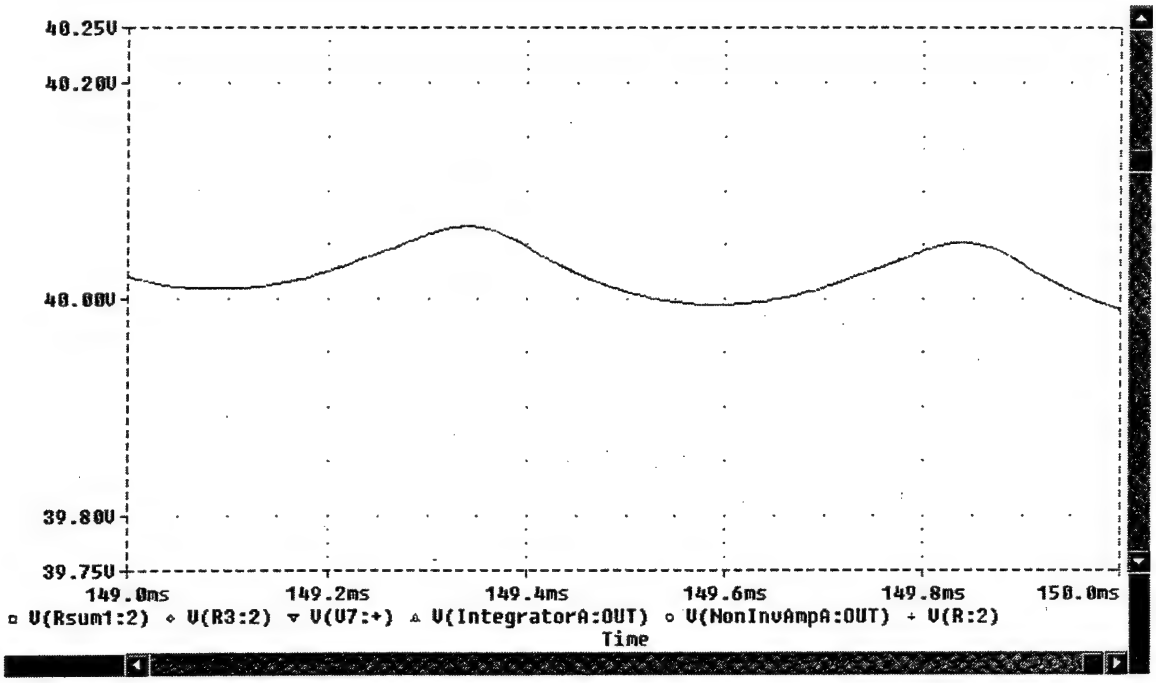

Figure VII-10 Commanded 40V Output Voltage Ripple

2. Load Test

Further testing of the two-switch control consisted of varying the load resistance. Load values were varied by 25% to establish the ability of control to operate under varying load conditions. Test simulations demonstrated excellent results. The value of 'R' is now changed to 5 ohms to demonstrate a 74% decrease in load.

The circuit in was simulated in PSPICE with the new load value. The output voltage is shown in Figure VII-11 along with a look at the output of three of the 741 operational amplifiers. The output voltage homes in on the commanded 40V approximately 20ms faster than with a 19.3 ohm load. For heavy load conditions, the value of capacitor 'C' will require careful increase in value to ensure the desired minimal ripple is placed across the load.

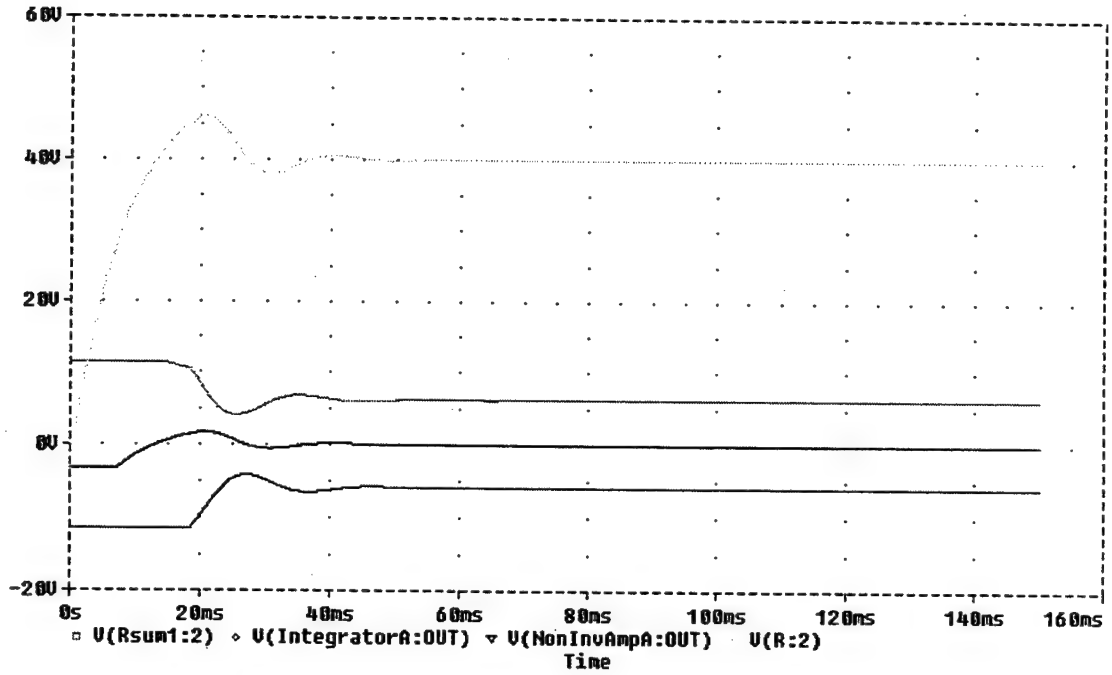

Figure VII-11 Commanded 40V Output with 5 Ohm Load

Next, the output voltage ripple is shown in Figure VII-12. Again the ripple is < 0.2% at 149ms.

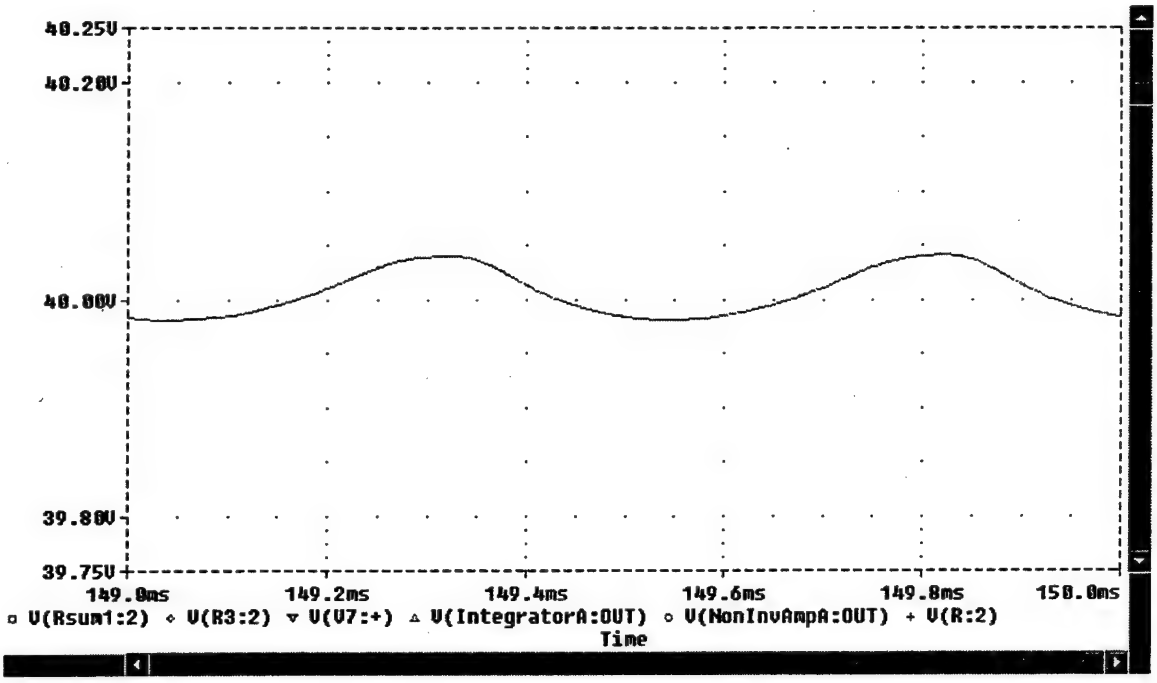

Figure VII-12 Commanded 40V Output Voltage Ripple with 5 Ohm Load

VIII. CONCLUSIONS

A. SUMMARY OF FINDINGS

Many applications exist for soft-switching converters. DC-to-DC converters were categorized here according to application and efficiency. Many different topologies exist that are capable of filling those applications and efficiency needs. The most efficient topologies were examined and presented on a similar level to allow for comparisons to be made.

Based on desires to meet future high-voltage requirements with a single source, the Joung topology was selected. Joung's topology offered the highest efficiencies and the most straightforward analysis. Each mode of operation was described and equations were developed to model them. PSPICE analysis was utilized to confirm the expected outputs. PSPICE was also used to validate the proper operation of the proportional plus integral control design. PSPICE simulation presented the expected and the unexpected nuances of the control. The unexpected factor being the sensitivity of the optical isolators.

The overall results are promising for the application of a high-voltage model. The circuit operates as expected and the feedback control is stable.

B. FUTURE WORK

In the future, more emphasis should be placed on the insertion of optical isolators with better current handling capabilities and current transfer ratios to avoid the nuances of convergence errors discovered here in PSPICE.

The controller designed in this work was built but not tested. The first subsequent effort should be to complete the bench testing within the lab for the low-voltage model developed here. The application of the low-voltage modeling should prove invaluable to the student attempting to develop the high-voltage model.

If future controllers incorporate mixed logic design, sufficient time should be allotted for the learning curve associated with the available version of ORCAD's schematic capture PSPICE version 9.1. The transformation from MicroSim's version 8 is not straightforward and will require dedicated time.

High-voltage modeling will require the insertion of totally new switches in order to handle the voltages. Stray capacitance and inductance will also have to be considered in future modeling and bench testing.

APPENDIX A: MATLAB CODE

A. DESIRED POLES

```
% Clifton Turner
% 27 July 1999
% A determination of the best gains (Ki and Kp) and
%Capacitor %(C) in order to produce a stable controller.

% A program that ask the user for the values of the desired
% locations of the poles for a controller who's closed loop
% system response is given by:

% CLR = (Ki*E + (Kp*E)s)/(Ki*E + (Kp*E + 1)s +(L/R)s^2 +
(L*C)s^3

% The program returns the Capacitor(C) and Gains(Kp & Ki)
% required to obtain the desired values.

% The program runs until the user is happy with the results
% obtained.

% Place the result at the top of a clear screen.

clear all

term = 1;
while term == 1,
  a = input('Enter the factor times -1000 desired --> ')
  b = input('Enter the factor times -500 + 866i desired -->
')
  c = input('Enter the factor times -500 - 866i desired -->
')
  disp(' ')

  % Declare all constants
  E = 50.8;
  C = 90e-6;
  L = 42.5e-3;

  % POLE Specifications
```

```
  The_poles = [a*(-1000), b*(-500+866i), c*(-500-866i)];
  S = poly(The_poles);


  % Gain Calculations
  R = 1/(C*S(2))
  Ki = L*C*S(4)/E
  Kp = (L*C*S(3)-1)/E

  % Formulas that describe the closed loop controlled system
  num = [Kp*E Ki*E];          % Allows the zero
specification
  den = [L*C L/R Kp*E+1 Ki*E]; % Allows the pole
specification



  % Check the new pole locations
  poles_check = den/(L*C);
  Pole_roots = roots(poles_check);

  % Check the Zero location
  NUMroots = roots(num)

  Denominator_Roots = roots(den)
  plot(Denominator_Roots, 'bd')

  term = input('To continue enter 1  To quit enter 0 ');
  disp(' ')
end   %while loop

disp('Carry On ')
```

B. DESIRED POLE RESULT

```
Enter the factor times -1000 desired --> 1.33

a =

    1.3300

Enter the factor times -500 + 866i desired --> 1.33
```

```
b =

    1.3300

Enter the factor times -500 - 866i desired --> 1.33

c =

    1.3300


R =

    4.1771

Ki =

  177.1347

Kp =

    0.2467

NUMroots =

 -718.0493


Denominator_Roots =

  1.0e+003 *

  -1.3300
  -0.6650 + 1.1518i
  -0.6650 - 1.1518i

To continue enter 1  To quit enter 0
```

C. CAPACITANCE NEEDED TO OBTAIN DESIRED LOAD

```
% This .m file (BuckRipple.m) calculates the capacitor value
required
% given the %Ripple desired in a Buck chopper circuit.

% Clifton Turner
% 29 July 1999

% The user enters values for the source voltage, Load
resistance,
% Inductance, & desired load voltage.  The program returns
the
% minimum required value for the load capacitance (Vc) for
% a standard Buck chopper circuit.

clc
clear
close

DoAnother = 1;
while (DoAnother == 1)

 % get inputs
 E = input('Enter the value of the source voltage in volts -
-> ');
 disp(' ')
 R = input('Enter the value of the load resistance in ohms -
-> ');
 disp(' ')
 Vc = input('Enter the desired load voltage in volts --> ');
 disp(' ')
 L = input('Enter the value of the inductance in henrys -->
');
 disp(' ')
 f = input('Enter the desired switching frequency in hertz -
-> ');
 disp(' ')
 deltaVc = input('Enter the minimum desired peak to peak
ripple in volts --> ');


 % calculate the period T
 T = 1/f;
```

```
 % calculate the duty cycle
 D = Vc/E;

 % calculate Imin & Imax
 Imin = D*E*((1/R) - ((1-D)*T)/(2*L));
 Imax = D*E*((1/R) + ((1-D)*T)/(2*L));

 % calculate peak to peak value of capacitor voltage ripple
 Q = (Imax - Imin)*T/8;
 C = Q/deltaVc

 % determine if user wants to do another calculation
 DoAnother = input('Enter 1 to do another calculation -->
');
end % while DoAnother
```

D. NECESSARY CAPACITANCE RESULTS

Enter the value of the source voltage in volts --> 50.8

Enter the value of the load resistance in ohms --> 19.3

Enter the desired load voltage in volts --> 20

Enter the value of the inductance in henrys --> 42.5e-3

Enter the desired switching frequency in hertz --> 2000

Enter the minimum desired peak to peak ripple in volts --> .1

C =

8.9162e-005

LIST OF REFERENCES

[1] Petry, C. and Rumberg, J., "Zonal Electrical Distribution Systems: An Affordable Architecture for the Future," *Naval Engineers Journal*, v. 105, pp. 45-51, May 1993.

[2] Ashton, R.W., "TS3000 Electrical Power Engineering, "Class Notes" Naval Postgraduate School, Monterey, CA, October 1998.

[3] Fisher, M.J., *Power Electronics*, PWS-Kent Publishing Co., Boston, Massachusetts, 1991.

[4] de Freitas, L.C. & Gomes, P.R.C., "A High-Power High-Frequency ZCS-ZVS-PWM Buck Converter Using A Feedback Resonant Circuit," *Proc. of IEEE Power Electronics Specialists Conference*, pp. 330-336, 1993.

[5] Carlos, L., Ferreira, D. & Farias, V.J., "A Novel ZCS-ZVS-PWM DC-DC Buck Converter For High Switching Frequency: Analysis, Simulation and Experimental Results," *Proc. of IEEE Applied Power Electronics Conference and Exposition*, pp. 693-699, 1993.

[6] Hey, H.L., Matias, L. & Vieira, J.B., "A Buck ZC-ZVS PWM Converter," *Proc. of IEEE Power Electronics Conference and Exposition*, pp. 1379-1384, 1994.

[7] Mizoguchi, T., Ohgai, T. & Ninomiya, T., "A Family of Single-Switch ZVS-CV DC-to-DC Converters," *Proc. of IEEE Power Electronics Specialists Conference*, pp. 1392-1398, 1994.

[8] Chau, K.T., "A New Pulsewidth-Modulated Zero-Voltage-Switching Multi-Resonant Converter Using Resonant Inductor Freewheeling," *Proc. of IEEE Applied Power Electronics Conference and Exposition*, pp. 984-990, 1994.

[9] Prado, R.N., "A New ZVT PWM Converter Family: Analysis, Simulation and Experimental Results," *Proc. of IEEE Applied Power Electronics Conference and Exposition*, pp. 978-983, 1994.

[10] de Freitas, L.C. & Gomes, P.R.C., "A High-Power High-Frequency ZCS-ZVS-PWM Buck Converter Using A Feedback Resonant Circuit," *Proc. of IEEE Power Electronics Transactions*, pp. 19-24, 1995.

[11] Dananjayan, P. & Chellamuthu, C., "A New Constant Frequency Zero Voltage Switching Buck Quasi-Resonant Converter," *Proc. of IEEE Power Electronics, Drives and Energy systems for Industrial Growth Conference*, pp. 176-182, 1995.

[12] Joung, G.B., "New Soft Switched PWM Converter," *Proc. of IEEE Power Electronics Conference and Exposition*, pp. 63-68, 1996.

[13] Grigore, V. & Kyyra, J., "A New Zero-Voltage-Transition PWM Buck Converter," *Proc. of IEEE Mediterranean Electromechanical Conference*, pp. 1241-1245, 1998.

[14] Ciezki, J.G. & Ashton, R.W., "Analysis of a PWM Resonant Buck Chopper for Use as a Ship Service Converter Module," Naval Postgraduate School, Monterey, CA, January 1999.

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